Total Ionizing Dose in Nano-Scaled CMOS Technologies

Federico Faccio, *Member, IEEE*, Giulio Borghello, *Member, IEEE*, and Stefano Bonaldo, *Senior Member, IEEE*

***Abstract*—Despite incredible technological advances in the fabrication of MOS transistors, the widespread use of isolation layers makes the total ionizing dose (TID) a persistent threat to the operation of these devices in ionizing radiation environments. This article provides a comprehensive review of the past three decades of research on the TID effects in transistors built across various scaled complementary metal-oxide-semiconductor (CMOS) nodes, ranging from a 1.6-μm planar MOS field-effect transistor (MOSFET) technology to FinFETs produced in a 16-nm node. The focus is on understanding the evolution of the TID effects with the scaling down, as different oxides and channel layouts are employed in the CMOS processes.**

***Index Terms*—Complementary metal-oxide-semiconductor (CMOS) technology, MOS field-effect transistor (MOSFET) reliability, shallow trench isolation (STI), spacer oxides, total ionizing dose (TID), ultra-high doses.**

I. Introduction

OVER the past 50 years, complementary metal-oxide-semiconductor (CMOS) technologies have emerged as a major driver of innovation in the field of advanced and complex integrated circuits and have gradually grown to dominate the electronics market. However, when exposed to radiation, circuits based on MOS field-effect transistors (MOSFETs) fabricated in a CMOS process can exhibit deviations from their nominal operation. Among the different radiation-induced phenomena that can affect the performance of MOS devices, this article focuses on the effects produced by total ionizing dose (TID). This is a cumulative effect, meaning that it requires the accumulation of radiation-induced defects before the device malfunctions.

The sensitivity of CMOS technologies to TID effects was identified as early as the 1960s [1], when accumulation of charge in the gate oxide of MOS transistors exposed to ionizing radiation was found to be responsible for significant threshold voltage shifts and consequent circuit failure. Extensive research over the course of several decades has demonstrated that radiation-induced charge is retained within the oxide due to the presence of trapping centers located in the bulk of the oxide [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12] and at the Si/SiO_2 interface [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36]. Although CMOS technologies have considerably evolved since the 60s—first shrinking their size in planar technologies following Dennard's down-scaling law [37], and more recently shifting to the 3D FinFET technologies, where the conduction channel is surrounded by the gate on three sides—the presence of SiO_2 remains pervasive even in the most advanced nodes, making MOS transistors inherently sensitive to TID effects.

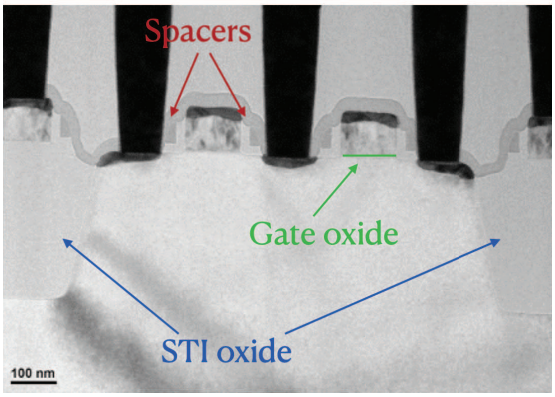

Fig. 1. TEM image of a real CMOS technology highlighting the same oxides. Here, two transistors sharing the same central diffusion are visible.

Among the numerous insulators employed in CMOS technologies, three stand out as being responsible for all the degradation mechanisms observable during and/or after irradiation. These insulators are highlighted in Fig. 1, which shows a transmission electron microscopy (TEM) image of the physical implementation of an MOS transistor with the insulator layers surrounding it, and are listed hereafter[1]:

- *Gate Oxide Stack:* It is typically a very thin layer (below 5 nm for CMOS nodes smaller than 250-nm) always fabricated in high-quality thermally grown SiO_2 and/or high-k dielectric materials with low defect and interface trap densities.
- *Shallow Trench Isolation (STI) Oxide:* It is typically fabricated in low-quality (high defect density) deposited SiO_2 and is located around the transistor to isolate it from nearby devices.

[1]This article does not address SOI technologies, in which the buried oxide (BOX) is frequently the primary factor contributing to the TID sensitivity of the device.

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- *Spacers:* They are typically fabricated in low-quality deposited SiO_2 and Si_3N_4 and are located in the lateral regions of the gate oxide to allow the implantation of the lightly doped drain/source (LDD) regions.

Although these oxides differ in terms of quality and location, the basic mechanisms ruling the transport and trapping of charge in SiO_2 are essentially the same regardless of the function of the oxide layer. Therefore, the vast literature describing the dynamics of charge transport and trapping, often initially developed for phenomena happening in the gate oxide, remains valid also for other SiO_2 layers [38], [39], [40], [41], [42], [43], [44], [45], [46], [47], [48], [49], [50], [51], [52], [53], [54], [55], [56], [57], [58], [59], [60], [61], [62], [63], [64], [65], [66], [67], [68], [69], [70], [71], [72], [73], [74], [75]. However, due to their differences in quality and location, each of these oxides leads to different device- and circuit-level responses in a radiation environment.

This work aims to review the TID effects and the underlying degradation mechanisms in MOS devices, organized by the oxide responsible for degradation (gate oxide, STI, and spacers). With respect to previous review papers, the impact of radiation on the STI and spacer insulators in CMOS technologies of the last 25 years is highlighted, summarizing the rich recent literature on the subject and providing a comprehensive framework to understand the origin of transistors' parametric shift that is no longer traceable to degradation in the gate oxide anymore. Most of this literature reports effects occurring "up to ultra-high doses," referring to doses that significantly exceed 10 Mrad(SiO_2), as encountered in some high-energy physics experiments. These dose levels can be significantly higher than those typical of space applications, whether in satellites or deep-space probes. For example, in the CERN High-Luminosity Large Hadron Collider (HL-LHC)—an upgraded version of the LHC, currently the most powerful proton accelerator in the world—electronic systems located in the proximity of the proton-proton collision point can be exposed to TID levels up to 1 Grad(SiO_2) over their operational lifespan [76]. However, original data presented in Section VI will demonstrate that TID in STI and spacer oxides also sensibly affect the transistors' electrical parameters at doses of interest for applications in space. The discussion will also address how effects resulting from trapped charge in auxiliary oxides make the TID response of modern technologies susceptible to true dose-rate (DR) effects, a phenomenon previously considered exclusive to bipolar transistors. This article concludes with an evaluation of the trends observed over the last 30 years in the TID sensitivity of commercial CMOS technology nodes.

II. Gate Oxide

A. Effects From Charge Trapping in the Gate Oxide

The accumulation of trapped charge in the gate oxide and at its Si/SiO_2 interface causes drifts in the electrical response of transistors exposed to ionizing radiation. TID-exposed Si MOSFETs with SiO_2 gate dielectric can trap positive charge in the gate oxide due to ionization-induced hole generation and proton release (H_+). This trapped positive charge in the gate oxide affects the transfer characteristics (dc static I_D-V_{GS}) of the transistors, as shown in Fig. 2.

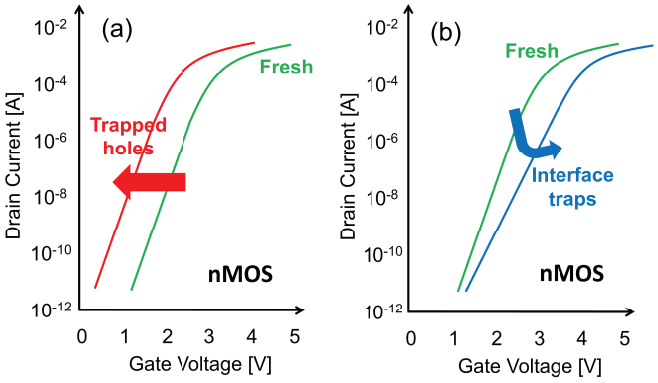


Fig. 2. Representative conceptual examples (not real measurements) of the TID effects induced by charge trapping in the gate oxide on the transfer characteristics (I_D-V_{GS}) of an nMOSFET. (a) Positive charge trapping in the gate oxide and (b) interface traps. The green curves refer to the as-manufactured (fresh) characteristics, the red curve represents the effect of holes trapped in the oxide, and the blue curve represents the effect of interface traps.

In nMOSFETs, positive trapped charges attract electrons from the silicon bulk toward the Si/SiO_2 interface, whereas in pMOS, they repel the holes from the interface. As a result, in both types of transistors, holes trapped in the oxide cause a rigid horizontal left shift of the I_D-V_{GS} curve, resulting in a measurable negative shift in threshold voltage [9], [10], [67]. In principle, for transistors having thick gate oxide (>10 nm), this V_{TH} shift (ΔV_{ot}) follows the relation:

$$\Delta V_{ot} = \frac{t_{ox}^2}{k_{ox}\epsilon_0} q \Delta N_{ot} \tag{1}$$

where ΔN_{ot} is the volumetric density of the positive trapped charge (cm^{-3}), t_{ox} is the thickness of the gate oxide, k_{ox} is the relative permittivity of gate oxide ($k_{SiO_2} \approx 3.9$), and ϵ_0 is the vacuum permittivity [77]. Thus, ΔV_{ot} is proportional to the volumetric density of trapped charge and increases with the square of the gate oxide thickness.

On the other hand, the polarity of the charge trapped in interface traps differs in nMOS and pMOS transistors and depends on the energy position of the trap in the bandgap relative to the Fermi level at the interface [17], [78]. The microscopic defects at the interface are typically related to silicon dangling bonds at the interface, called historically P_b centers. These defects behave as donor-like when their energy level is below the Si midgap and acceptor-like when above it [17], [78]. Donor-like defects are neutral below the Fermi level and become positive above it, releasing an electron. In contrast, acceptor-like defects are neutral above the Fermi level and become negative below it, capturing an electron. Since the Fermi level at the interfaces moves with the gate voltage, the charge state of interface traps also changes with V_{GS} and is neutral when $E_{Fermi} = E_{Midgap}$ [78], [79]. When the transistor is brought in the inversion region and the channel starts to appear, charge gets trapped in the P_b centers (electrons in nMOSFETs and holes in pMOSFETs) and this leads to a stretch of the I_D-V_{GS} curves in the subthreshold region [Fig. 2(b)] and a

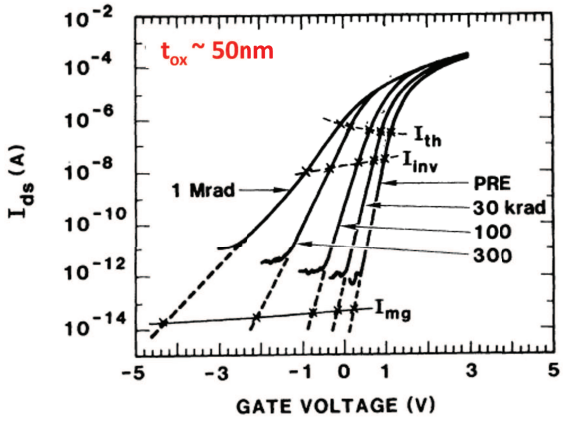


Fig. 3. Transfer characteristics of an nMOS transistor of considerable gate oxide thickness (50 nm) irradiated to 1 Mrad(SiO_2) with V_{DS} = 10 V. Markers evidence the currents corresponding to threshold (I_{th}), inversion (I_{inv}), and midgap (I_{mg}). The plot highlights the TID-induced degradation from the positive charge trapped in the gate oxide that leads to the left shift of the curve at midgap (I_{mg}). The very visible increase of the subthreshold swing is instead due to activation (depassivation and charge trapping) of interface traps. (After [79].)

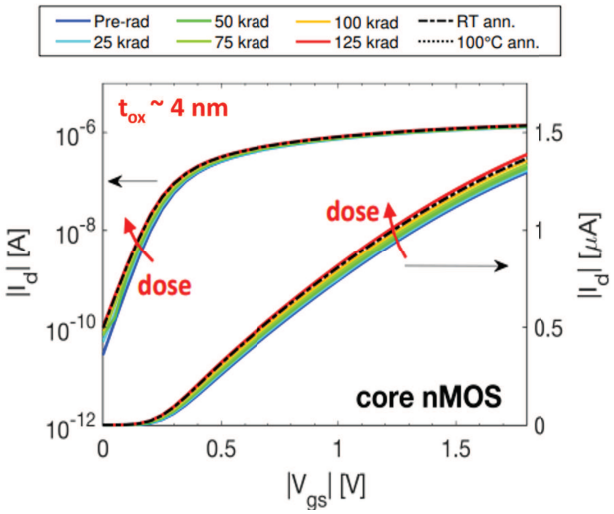


Fig. 4. Degradation of I_D-V_{GS} in linear region (V_{DS} = 0.1 V) of nMOSFETs fabricated in the 150-nm technology node, having a gate oxide thickness of about 4 nm. The transistor was irradiated at room temperature up to 125 krad(SiO_2) and then annealed for 24 h at 100 °C with V_{GS} = 0.9 V. (After [86].)

consequent shift in V_{TH}. While for the nMOSFETs, the trapped electrons can compensate the effect of holes trapped in the oxide, in pMOSFETs, holes are also trapped at the interface and their effect adds to a more severe TID degradation. Other than the V_{TH} shift, interface traps also induce a degradation of the transconductance (g_m), which may be measured as a loss of the maximum g_m when the transistors operate in the linear regime. This effect is induced by the greater scattering generated by the interface traps on the channel carriers.

Fig. 3 illustrates the typical TID response of an n-channel MOSFET with a thick gate oxide (about 50 nm). As the accumulated dose increases, the I_D-V_{GS} curve in logarithmic scale shifts left due to the rising density of positive charge trapped in the gate oxide. This is clearly visible looking at the gate voltage for I_{mg}, the current at midgap where interface traps are neutral. Moreover, the I_D-V_{GS} curves stretch in the subthreshold region due to the TID-induced activation of interface traps. Notably, when the channel is in inversion, negatively charged interface traps partially compensate for positive trapped holes in the gate oxide (voltage shift at I_{th} is considerably smaller than at I_{mg}). The contributions to the V_{TH} shift from charge in both gate oxide and interface traps can be extrapolated by evaluating the shift at midgap and the stretch-out of the subthreshold swing, as detailed in [40].

B. Oxide Thickness Dependence

The constant down-scaling of CMOS technologies driven by Moore's law [80], [81] has entailed a proportional decrease of the SiO_2 gate thickness, which resulted in an improved resilience of the gate oxide, thus of analog and digital Integrated Circuits (ICs), to TID effects [9], [10], [67], [73]. For example, Fig. 4 shows the TID response of a relatively recent nMOSFET fabricated in the 150-nm technology node with a SiO_2 gate oxide of about 4 nm. The logarithmic scale curves (left bundle) evidence very limited left-shift compared to those in Fig. 3 for a much thicker oxide. This

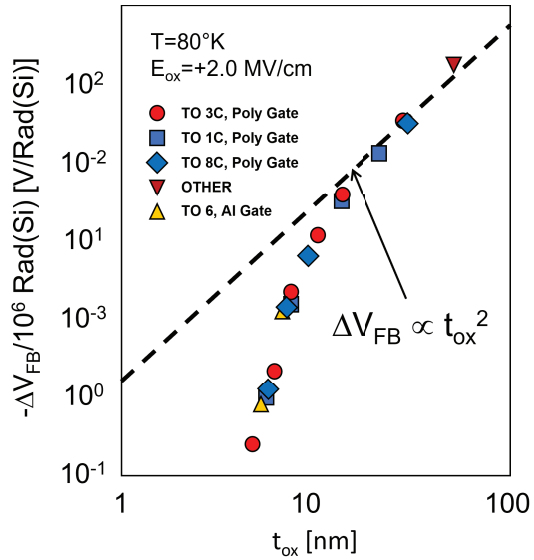


Fig. 5. Flatband voltage shift per unit dose as a function of gate oxide thickness in MOS capacitors irradiated at 80 K with ^{60}Co γ-rays. The dashed curve indicates the assumption of t_{ox}^2 dependence [85] for thick gate oxides. (After [82].)

difference originates in ΔV_{ot} proportionality to t_{ox}^2 expressed by (1) and experimentally confirmed by the data plotted for MOS capacitors in Fig. 5 [82], [83]. Measurements were performed at very low temperature to "freeze" holes at their generation and prevent the formation of interface traps [84]. In these conditions, the radiation-induced shifts in flatband and threshold voltage are solely due to charge trapped in the oxide. For thicknesses > 10 nm, the flatband voltage shift per unit dose decreases with a trend proportional to t_{ox}^2 [85]. However, for thicknesses < 10 nm, the reduction in hole trapping occurs much faster than the expected t_{ox}^2 dependence visible in thicker oxide capacitors [73],

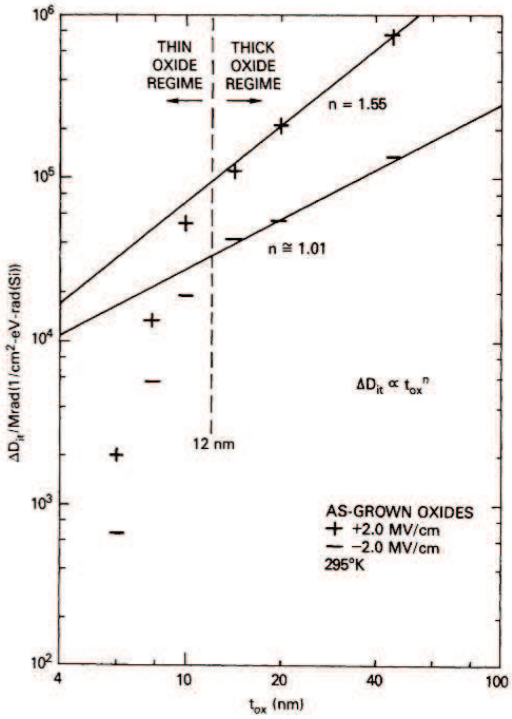


Fig. 6. Density of interface traps per unit dose and energy D_{it} as a function of gate oxide thickness in MOS capacitors irradiated with ^{60}Co γ-rays with two different electric fields during exposure: ± 2 MV/cm. Considerably higher densities are observed during irradiation at positive bias, conformal with drift of the generated and released H_+ in the oxide toward the gate Si/SiO_2 interface, where it depassivates Si–H bonds and activates interface traps. (After [87].)

[82], [83]. This abrupt decrease in hole density is related to their recombination with tunneling electrons, neutralizing trapped holes near the metal/oxide or oxide/semiconductor interfaces within approximately ~3 nm. Thus, the validity of (1) is limited to transistors fabricated in technologies with gate oxide thicker than 10 nm. In case of transistors with extremely thin oxides, as commonly used in modern core transistors, the actual ΔV_{ot} may be lower than the value calculated using (1).

The relationship between gate oxide thickness and radiation-induced generation of interface traps follows a similar trend. Fig. 6 reports the density of interface traps per unit dose as a function of oxide thickness in several MOS capacitors [87]. Also, in this case, an abrupt reduction in the interface-trap density is observed in ultra-thin oxides < 10 nm. Tunneling electrons from the metal/oxide or oxide/semiconductor interfaces neutralize trapped holes in the oxide, preventing the release of H_+ responsible for the interface traps buildup. Moreover, as indicated by "+" markers, a positive electric field efficiently drives the H_+ ions toward the Si/SiO_2 interface, thereby increasing the density of interface traps compared to the one of negative electric fields indicated by "−" markers [14], [29], [50], [87].

Because of the above, the reduction of the gate oxide thickness accompanying CMOS scaling has strongly benefited the radiation resilience of modern MOSFETs [73], [88]. However, TID effects have become more complex with the introduction of high-k gate materials and alternative materials and structures in modern semiconductor technologies [73], [89]. Concerning the gate material, the 65-nm technology was one of the last nodes using ultra-thin SiO_2 layers (about 1.5 nm to 2 nm). Starting from the 45-nm node, the scaling limits of SiO_2 have required the introduction of high-k dielectric materials, with hafnium dioxide (HfO_2) being the overwhelming dominant choice. However, this required the use of a stack where the high-k material is on top of an ultra-thin SiO_2 layer (<1 nm) in contact with the Si channel. This layer mitigates issues related to lattice mismatches and reduces defect formation at the semiconductor/oxide interface, benefiting from robust fabrication processes that involve the growth of SiO_2 on Si substrates. As a consequence, the introduction of high-k dielectric resulted, in Si-based MOSFETs, in a very limited change in TID tolerance [90], [91], [92], [93], [94], [95], [96]. However, the above described improvement of the TID tolerance of scaled-down Si-based CMOS technologies may not extend to transistors fabricated in other materials, e.g., III-V compounds. In III-V transistors, lattice mismatch at material interfaces and the integration of high-k dielectrics can significantly influence the TID sensitivity [97], [98], [99], [100], [101], [102], [103], [104].

C. Border Traps and Low-Frequency Noise

Other than influencing the threshold voltage, radiation-induced traps in the gate SiO_2 can exchange charge with the channel and, in so doing, generate excess noise in the transistor's current. Since the neutralization likelihood of a hole trapped in the gate oxide by an electron from the silicon bulk depends on the distance between the oxide trap and the Si/SiO_2 interface [105], only traps near the interface exchange electrons quickly, also depending on the applied electric field [8]. Traps within about 3 nm of the interface, known as "border traps," can exchange electrons with the Si substrate with emission and capture times in the range between 0.01 and 1 s [57], [105], contributing to low-frequency noise (LFN) [8], [54].

The LFN of MOS transistors is typically related to fluctuations in carrier number [74], [106] and is significantly influenced by fabrication processes and technology node. Charge exchange can occur between the device channel and border traps through tunneling and thermally assisted processes [57], [71], [74], [107], [108]. LFN has been experimentally evaluated in several MOS transistors by monitoring drain-current (I_D) or drain-voltage (V_{DS}) fluctuations over time under constant bias conditions. For constant V_{GS} and V_{DS}, the drain current can be expressed as $I_D(t) = \bar{I} + i(t)$, where $\bar{I}$ is the average drain current and $i(t)$ represents random fluctuations over time [109], resembling the signal shown in Fig. 7(a) [95]. The current signal is sampled in the time domain and then converted to the frequency domain using the discrete Fourier transform (DFT), from which the power spectral density (PSD) is calculated. In the linear region of device response, the drain-current noise PSD S_{id} is related to the drain-voltage noise PSD S_{vd} by the relation [74], [110], [111], [112]

$$S_{vd} = R_{ch}^2 S_{id} = \frac{V_{ds}^2}{I_{ds}^2} S_{id} \tag{2}$$

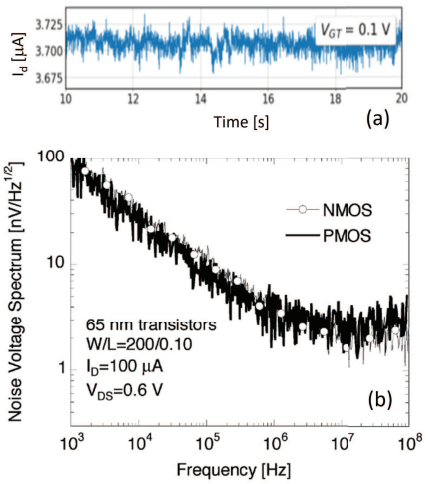


Fig. 7. (a) Drain current signal in the time domain of a Si transistor biased with the channel in inversion at constant $V_{gt} = V_{GS} - V_{TH} = 0.1$ V and $V_{DS} = 50$ mV. (b) Drain-voltage noise spectrum of nMOS and pMOS transistors fabricated in a 65-nm CMOS node, at constant current bias $I_D = 100$ μA. (After [95] and [113].)

where R_{ch} is the channel resistance, calculated as the average drain current I_{ds} divided by V_{ds}. The PSD of the drain voltage S_{vd} (or of the drain current S_{id}) of a Si-based FET is typically proportional to $1/f$ at low frequency (flicker noise) and constant (white noise) at high frequency, as shown in Fig. 7(b) for pristine nMOS and pMOS transistors fabricated in a 65-nm CMOS technology. The $1/f$ noise and the white noise due to the thermal and shot noise components are clearly visible, with a transition at $f \approx 1$ MHz [113]. To first order, neglecting mobility fluctuations, the drain-voltage noise PSD (S_{vd}) of MOS devices can be described by the number-fluctuation model [106], [114]

$$S_{vd} = \frac{q^2}{C_{ox}^2} \frac{V_{DS}^2}{(V_{GS} - V_{TH})^2} \frac{kTD_t(E_f)}{LW \ln(\tau_1/\tau_0)} \frac{1}{f} \tag{3}$$

where V_{TH} is the threshold and gate voltage; C_{ox} is the gate-oxide capacitance per unit area; L and W are the transistor channel length and width, respectively; $D_t(E_f)$ is the border-trap density at the Fermi energy E_f; T is the temperature; k is Boltzmann's constant; f is the frequency; and τ_0 and τ_1 are the minimum and maximum tunneling times, respectively [106].

After TID exposure, the generated border traps result in an increased LFN in Si MOSFETs [106], [115], [116]. Fig. 8 shows a case-study for an old micrometer-sized nMOSFET, which is irradiated with ^{60}Co γ-rays and always measured at the same gate voltage overdrive $V_{gt} = V_{GS} - V_{TH}$. The noise spectral density only covers the low-frequency range and exhibits the typical $1/f$ dependency. The evident increase in magnitude with TID is due to the buildup of border traps [114], [117]. A more recent example for a modern transistor fabricated in a 16-nm FinFET technology is shown in Fig. 9 [91], [96], [113], [118], [119], [120], [121]. The LFN has been measured before irradiation, at ultra-high doses [1 Grad(SiO_2)], and after 24 h of annealing at 100 °C [118]. The plots in Fig. 9(a) reveal a typical $1/f$ noise increase with TID, again indicating border trap generation. The slight

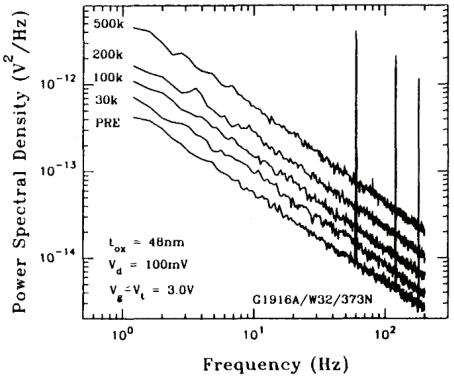


Fig. 8. $1/f$ voltage noise spectral density S_{vd} of n-channel Si MOSFET at $V_{GS} - V_{TH} = 3$ V. Devices were irradiated up to 500 krad(SiO_2) with ^{60}Co γ-rays, while $V_{GS} = 6$ V. (After [115].)

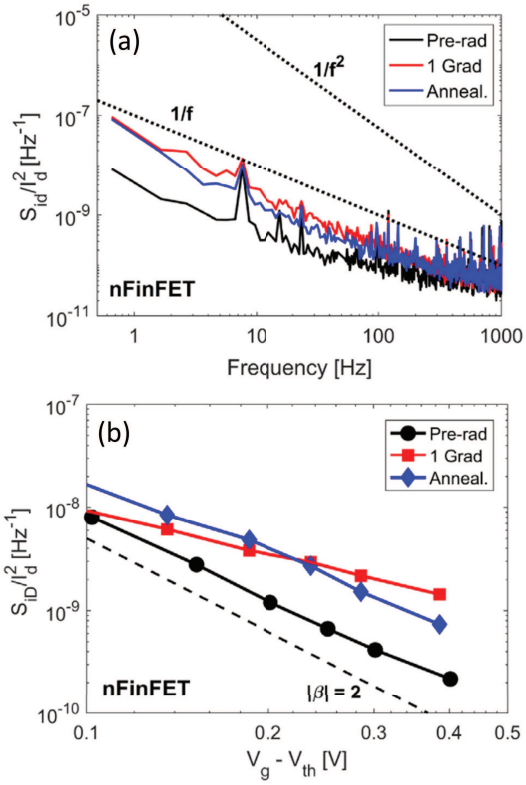


Fig. 9. (a) Normalized PSD of the drain current for transistors fabricated in a 16-nm FinFET technology at $V_{DS} = 50$ mV and $V_{GS} = 0.85$ V. (b) LFN current magnitude at $f = 10$ Hz versus $V_{GS} - V_{TH}$ at $V_{DS} = 50$ mV for the same transistors that were irradiated with X-rays up to 1 Grad(SiO_2) and then annealed for 24 h at 100 °C. (After [118].)

noise decrease after high-temperature annealing suggests their partial neutralization [8], [74], [106]. Notably, the increase is modest considering the ultra-high doses, demonstrating the robust TID response linked to the ultra-thin gate oxide layer in this down-scaled technology. Fig. 9(b) shows the noise magnitudes at $f = 10$ Hz measured at several gate voltage overdrive, $V_{gt} = V_{GS} - V_{TH}$. The $S_{id} - V_{gt}$ plot offers insights into the defect densities contributing to charge trapping, particularly through the slope β. When traps contributing to noise are distributed

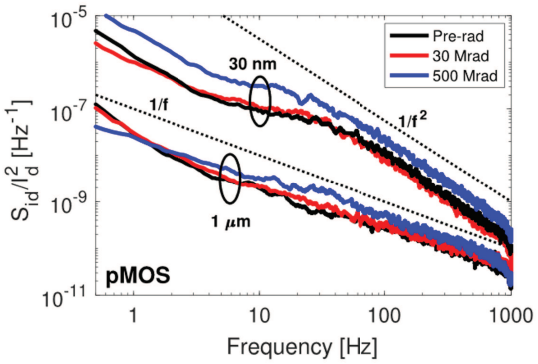


Fig. 10. Normalized PSD of the drain current for a pMOSFET fabricated in a 28-nm technology node irradiated with X-rays up to 500 Mrad(SiO_2). The noise was measured at $V_{DS} = -0.1$ V and $V_{GS} = -0.9$ V. (After [91].)

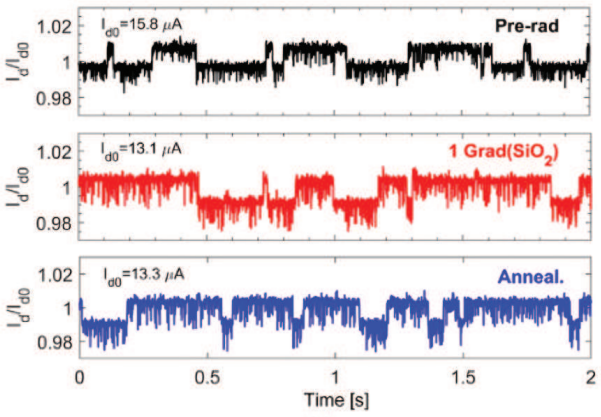


Fig. 11. RTN for a pFinFET fabricated with a 16-nm technology node with $L = 16$ nm, irradiated up to 1 Grad(SiO_2). (After [118].)

uniformly in space and in energy in the Si bandgap, the LFN is characterized by $\beta = 2$ (dashed line in the figure) [74], [106], [110], [111], [112]. Deviations from $\beta = 2$ indicate energetically and spatially non-uniform defect distributions. In Fig. 9(b), the fresh device exhibits a great uniformity in the trap distribution, which increases and becomes less uniform after irradiation [118].

As the technology scales down, LFN can become a significant concern because S_{vd} increases with decreasing channel size W and L [see (3)]. In nano-scaled devices, individual defects near the interface can dominate the overall LFN response, leading to random telegraph noise (RTN) [122], [123], [124], [125], [126], [127], [128], [129]. RTN is observable only in small devices due to the alternating capture and emission of carriers at specific defect sites, resulting in discrete switching in the device channel resistance. For charge capture and emission phenomena with a characteristic time constant τ, a single RTN fluctuation exhibits a Lorentzian PSD [95], [123], [124], [125]

$$S_{vd} = \frac{2\tau\Delta V_{DS}^2}{4 + (2\pi f\tau)^2} \tag{4}$$

where ΔV_{DS} is the V_{DS} fluctuation caused by the charge capture/emission at a prominent defect. Each prominent defect has a corner frequency [$f_c = 1/(2\pi\tau)$], indicating the frequency at which S_{vd} falls to half its plateau value. At frequencies $f \gg f_c$, the noise magnitude of S_{vd} falls off as $1/f^2$ for RTN [123], [124], [125]. This means that nano-scaled devices may exhibit LFN with a $1/f^2$ signature. Fig. 10 shows the results for two pMOSFETs fabricated in a 28-nm planar bulk Si technology, irradiated with 10 keV X-rays up to 500 Mrad(SiO_2) [91]. The long-channel pMOSFETs ($L = 1$ μm) show typical $1/f$ noise, while the short-channel pMOSFETs ($L = 30$ nm) show noise scaling with $1/f^2$. The LFN of the short-channel device identifies two different prominent defects that are stable along the irradiation, being characterized by Lorentzian distributions with corner frequencies $f_c < 1$ Hz for the slowest trap and $f_c \approx 30$ Hz for the fastest trap. Lorentzian distributions are typically found in small devices, which have short (small L) and narrow (small W) channels. Importantly, identical transistors from the same wafer and/or die may exhibit different Lorentzian distributions [91], [95], [118], [122].

Fig. 11 reports the LFN of the shortest pFinFETs ($L = 16$ nm) fabricated in a bulk FinFET technology. The device was irradiated with X-rays up to 1 Grad(SiO_2) and then annealed for 24 h at 100 °C [94], [118]. Before irradiation, the pFinFET exhibits RTN in the time domain, which is generated by a prominent pre-existing defect. The capture/emission time of the prominent trap is $\tau_c/\tau_e = 0.15/0.17$ s, which corresponds, in the frequency domain, to a Lorentzian power spectrum with $f_c \approx 6$ Hz. In this case, this prominent defect is stable throughout the TID irradiation and elevated-temperature annealing [122].

However, in some cases, defects have been found to be unstable. For instance, defect reconfiguration during irradiation has been reported in gate-all-around Si nanowire FETs [95], [96]. The LFN noise of these devices is dominated by prominent pre-existing defects located in the channel and/or very close to the gate oxide interface [74], [95], [96], [106]. Fig. 12 shows the S_{vd}–f curves for gate-all-around field-effect-transistors (GAA-FET) irradiated with 10 keV X-rays up to 2 Mrad(SiO_2) [95]. The pre-irradiation response in (a) displays multiple instances of RTN, characterized by different values of f_c, which vary with temperature [95], [96], [106]. After irradiation, the noise magnitude remains similar [Fig. 12(b)], but the defect-energy distribution is altered, as reflected by the different values of f_c. Tests on similar devices under ultra-high doses [96] show that the LFN response of short GAA-FETs can be dominated by prominent defects that redistribute in position and/or energy during irradiation. Their LFN response significantly varies from device-to-device [95], [96], [122].

Considering that typical border trap densities D_t in Si-based FETs with high-k dielectrics can be on the order of 1×10^{12} cm^{-2} and the channel area of nano-wires is in the order of 1×10^{-11} cm^2, a rough estimate of the number of traps is $N_t = D_t A \approx 10$ traps [130]. Thus, it is not surprising that RTN is often observed in the smallest transistors fabricated in the most scaled CMOS nodes [122].

While the origin of LFN has traditionally been attributed solely to border traps, recent re-evaluations of experimental results indicate that interface traps also contribute to low-frequency $1/f$ noise observed in irradiated MOS devices

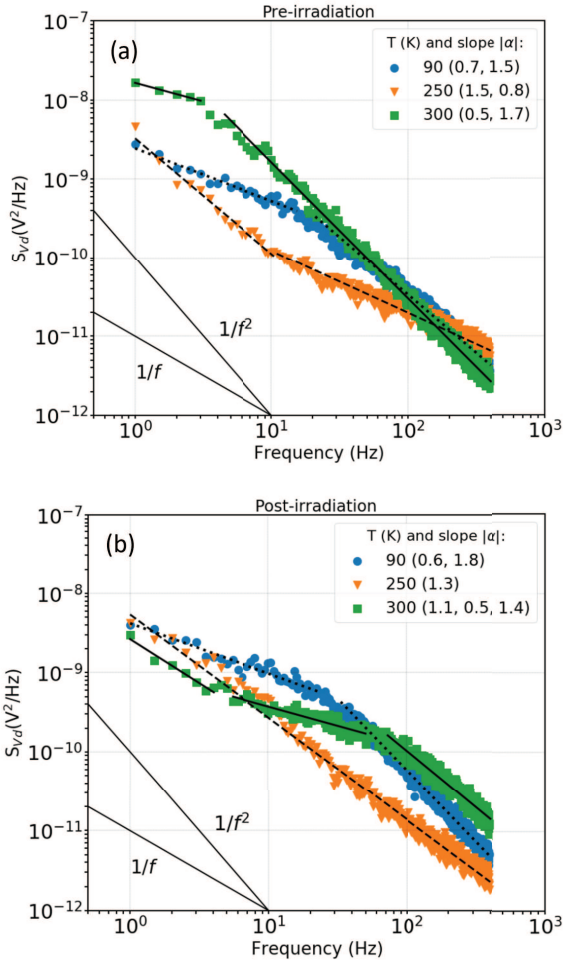


Fig. 12. LFN response at several temperatures of an FET built in the gate-all-around technology (a) before and (b) after irradiation with 10 keV X-rays up to 350 krad(SiO_2). Noise measurements were performed at V_{gt} = 0.4 V and V_{DS} = 50 mV. (After [95].)

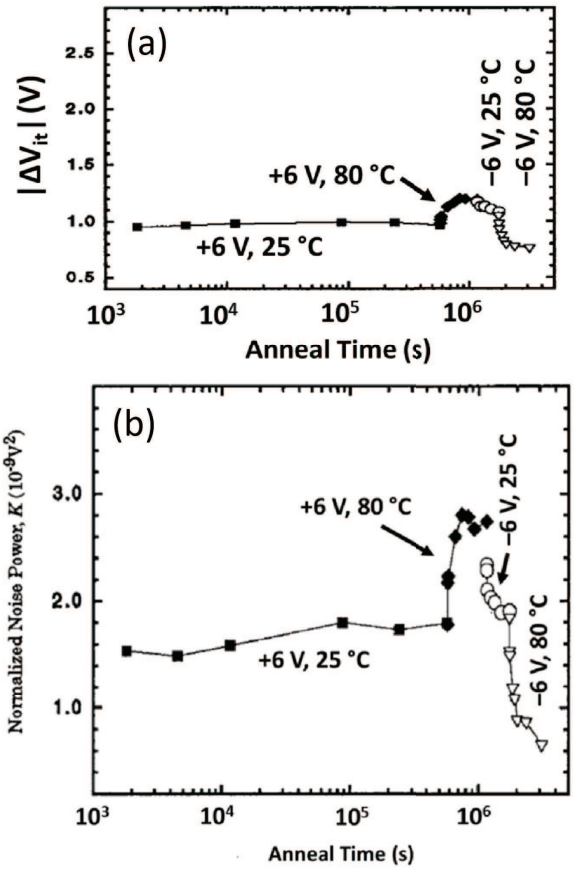


Fig. 13. (a) Variation of the threshold voltage induced by interface traps (ΔV_{it}). (b) Normalized LFN power (K) at 10 Hz. The measurements are retrieved for a pMOS transistor with ≈50 nm gate oxide thickness irradiated at 22 °C to 200 krad(SiO_2) with 10 keV X-rays and then annealed under several bias and temperature conditions as indicated in the plots (voltage values indicate V_{GS}). The solid (open) symbols denote positive (negative) bias anneals. (After [131].)

[132], [133]. Indeed, fluctuations in the noise can also be attributed to hydrogen-induced trap activation and passivation. Fig. 13 shows a significant example of great correlation between interface traps and LFN [131]. The plots show the V_{TH} shift induced by (a) interface traps and (b) LF noise response of pMOS transistors irradiated to 200 krad(SiO_2) and annealed under positive and negative bias. The positive bias used during irradiation enables the drift of H_+ toward the Si/SiO_2 interface, thus maximizing interface-trap buildup and facilitating comparisons of radiation-induced charge trapping and LFN. The V_{TH} shift induced by interface traps increases during 80 °C annealing at positive bias and decreases during negative-bias annealing [131] and is nicely correlated with the evolution of LFN. Results of these and other devices clearly show that annealing of interface traps, and not changes in border trap densities, leads to the observed response [107], [134]. Further studies at different temperatures allowed the understanding of the relevant hydrogen release, transport, and reaction processes leading to interface-trap activation and passivation, as well as their contributions to $1/f$ noise, in addition to that arising from border traps [132], [133].

III. STI Oxide

A. Drain-Source and Inter-Device Leakage Currents

Transistors in a planar CMOS technology are isolated by a thick oxide that, as of the 350-250-nm nodes, is manufactured with the STI technique—versus the local oxidation of silicon (LOCOS) used in older nodes. Unlike the gate oxide, which is thermally grown under specific controlled conditions to minimize the number of defects, the much thicker STI oxide is quickly deposited with techniques such as high density plasma chemical vapor deposition (HDP CVP). Sometimes, a thin thermal layer is grown after trench etching and before filling the trenches with the oxide. Grown oxides are normally rich in defects, which can lead to consistent charge trapping in a radiation environment and may lead to leakage currents in nMOS transistors (drain-to-source) and among n-doped regions (inter-device).

Fig. 14 shows an nMOS transistor surrounded by STI and, along two cut planes, the drain-source leakage current channel that can be activated by substrate inversion at its edges along the STI isolation. This leakage can thus flow even when the transistor is OFF (V_{GS} = 0 V). This situation is modeled by the addition of two "parasitic" transistors in parallel with the

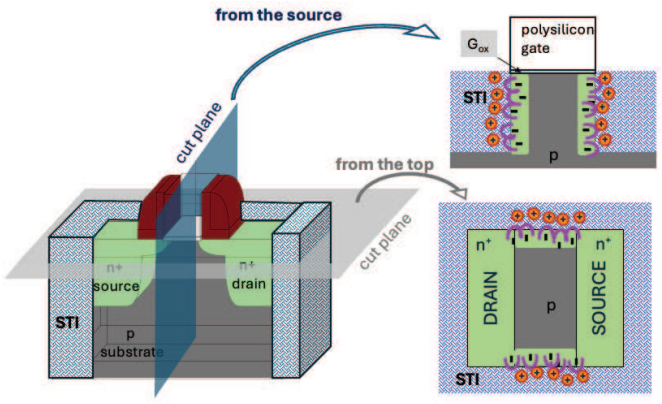


Fig. 14. View of the STI isolation surrounding an nMOS transistor along different cut planes, highlighting how radiation-induced trapped charge along the isolation border between source and drain might induce the creation of an inversion layer where current can flow. This happens only when hole trapping in the oxide (positive circles) is far superior to electron trapping (minus signs) in interface traps (purple horseshoes). Charge trapping is only shown where it matters for source-drain currents, but it happens in the whole of the STI oxide.

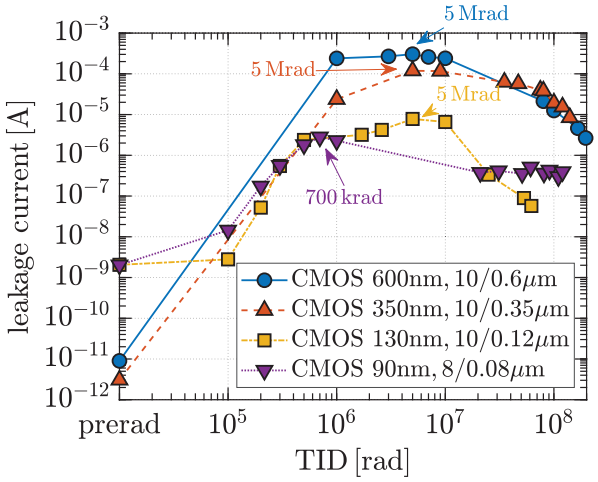


Fig. 15. Unpublished evolution of the drain-source leakage current during irradiation with X-rays (10 keV) at HDR (above 1 Mrad(SiO_2)/h) in sample nMOS transistors from four different CMOS technology nodes ranging from 600 to 90-nm. All samples exhibit a typical peak in the range of 1–10 Mrad(SiO_2), after which the leakage starts to decrease, while exposure is continued in the same conditions. All irradiation tests were done under bias (V_{GS} = V_{dd} and V_{DS} = 0 V) at HDR (above 1 Mrad(SiO_2)/h) and at room temperature and the source was an X-ray machine.

main one, with their gate voltages determined by the trapped charge in the STI. In reality, each of these two parasitic transistors consists of many transistors, whose equivalent gate oxide thickness is measured along the electric field lines, as illustrated in [135] for the older LOCOS technologies.

Only nMOS transistors are prone to TID-induced source-drain leakage current. In pMOS transistors, the positive charge trapped in the oxide and at the interface can only push the substrate further into accumulation, preventing the formation of a conduction channel that would require substrate inversion. Conversely, for nMOS transistors, the charge trapped in the oxide and interface traps has opposite polarity. Leakage current can only be observed when hole trapping far exceeds electron trapping, which is often the case for the fast qualification tests run in the lab at a DR much larger than in the application. However, the antagonist effect of the different charges, coupled to the different time and temperature dependence of the mechanisms leading to charge trapping, determines the non-monotonic evolution of the leakage current illustrated by the "rebound" of the leakage current shown in Fig. 15. Leakage is always measured at V_{GS} = 0 V and at the maximum drain-source voltage V_{GS} = V_{dd}. The contribution of a possible threshold voltage decrease to the leakage is not singled out, but, for a typical V_{TH} shift around or below 100 mV and a subthreshold swing of 80 mV/decade, it is limited in all cases to around or below 1 order of magnitude. Across all reported CMOS technology nodes, spanning from 600 to 90-nm, the evolution of the leakage current in nMOS transistors exhibits a peak around 2–10 Mrad(SiO_2). Note that these measurements were taken during a continuous exposure to X-rays at high dose-rate (HDR) and room temperature under bias, with periodic short interruptions to monitor the evolution of the transistors' characteristics. The leakage decrease is thus not attributable solely to annealing, but to the further TID accumulation. These curves are a small sub-set of results accumulated in the last 25 years in CMOS technologies covering nodes from 700 to 22-nm and are representative of the majority of the observed results. However, in the most recent technologies (starting from 130-nm), there are cases where no leakage appears in the whole range of TID explored, up to more than 100 Mrad(SiO_2) (this will be illustrated in Section VI).

The "rebound" in the leakage current of all transistors with TID in Fig. 15 is explained by the different evolution of trapping in oxide versus interface traps. Hole trapping in defect sites in the oxide is a fast mechanism; thus, accumulation of positive charge in the STI dominates the radiation response in the early stages of irradiation tests. When the amount of trapped charge is sufficiently large to bring a thin layer of the p-bulk silicon into inversion, a drain-source leakage current starts to flow at the edge of the transistor. The trapping of electrons at the Si/SiO_2 interface only occurs at a later stage since it requires depassivation of the interface traps by hydrogen (H_+) drifting through the oxide, which is a slow process. When this happens, the accumulation of trapped electrons gradually reduces the electric field in the inversion region, and the leakage current starts to decrease. This decrease is also fueled by the reduction in additional trapped holes at high TID due to the fact that most of the precursor trapping centers (e.g., oxygen vacancies) in the bulk of the STI oxide are already occupied [136].

Since charge trapping mechanisms depend on external variables such as DR, temperature, and applied bias (electric field), the evolution of the leakage current with TID can be very different when irradiation conditions are changed. Fig. 16 compares, on the same time scale, the leakage current in an nMOS transistor in the 130-nm node after a TID of 1 Mrad(SiO_2) but at two very different DRs (ratio >100). The fast irradiation produces an increase of the leakage by five orders of magnitude, versus only a factor of 10 for the

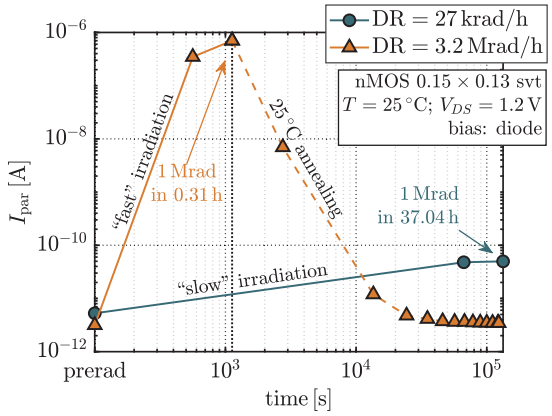


Fig. 16. Unpublished comparison of the drain-source leakage current (I_{par} = parasitic current) evolution of a minimum size nMOS transistor in the 130- nm node at two very different DRs. All other irradiation conditions were identical.

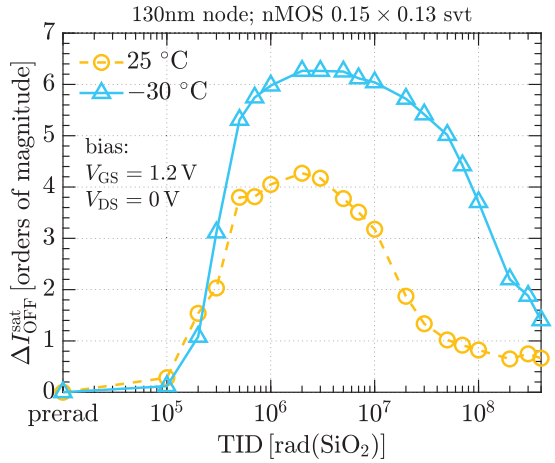


Fig. 17. Comparison of the leakage current evolution of an nMOS transistor at different temperatures. All other irradiation conditions were identical. The y-axis reports the increase in orders of magnitude with respect to the pre-rad value, where 1 means a 10× factor, 2 means a 100× factor, and so on. Data are for the same 130-nm technology as the one used in Fig. 16.

slow irradiation. This difference is entirely attributable to time effects: the longer time required for the low-rate exposure allows the slower depassivation of interface traps to happen, thus limiting the inversion of the parasitic channel close to the STI. At the same time, a portion of the holes trapped in the STI oxide can be de-trapped by thermal processes, reducing the amount of positive charge in the STI during the whole irradiation. Any change in T affects both the annealing of the oxide trapped charge and the drift of charge (holes and hydrogen) in the oxide, affecting the net increase of the leakage. This is clearly illustrated in Fig. 17, where more than two orders of magnitude separate the peak leakage current in nMOS transistors exposed at 25 °C or −30 °C. The presence and intensity of the electric field in the STI also strongly influence the initial charge yield and the movement of holes and hydrogen during the irradiation [70]. This determines a strong dependence of the resulting leakage current on the applied bias.

In light of all these strong influences on the leakage current evolution with TID, circuits can exhibit complex responses

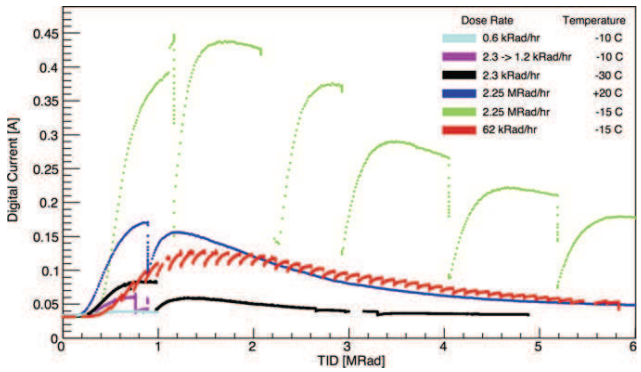


Fig. 18. Current consumption increase in the ABCstar ASIC during the qualification studies at different DRs and temperatures [137], [138]. Every discontinuity coincides with times when exposure was stopped while keeping the sample at the same temperature for some time. During these pauses in irradiation, annealing of trapped holes takes place and the leakage current decreases. After resuming exposure, freshly trapped holes increase the current consumption again. (After [137].)

during qualification and in the field, in particular when irradiation is not continuous. As a representative example, Fig. 18 reports the current consumption of the digital circuitry on the ABCstar application-specific integrated circuit (ASIC), a circuit designed for the ATLAS ITK (Inner Tracker) detector at the CERN Large Hadron Collider [137], [138]. Radiation tests took place at different T's and DRs, with frequent interruptions during which significant recovery was observed (while the temperature was kept constant). While annealing of trapped holes explains this recovery, each successive accumulation of holes when irradiation resumes brings the leakage to a smaller peak level. This is traceable to the accumulation of negative charge in depassivated interface traps, evidencing that these do not anneal significantly at the temperature of the test. Each of the test sequences with successive current peaks can be interrupted by a T increase beyond the point where fast annealing of interface traps happens, effectively resetting the device to pre-rad conditions. This was experimentally demonstrated in [139] on transistors in the same 130-nm technology, where the "reset" of the transistors to the pre-irradiation condition took place after an annealing step at 280 °C.

Although the leakage current evolution shown in Figs. 15, 17, and 18 is typical in most planar CMOS technologies, the details of the manufacturing process determine the energy level and the location of the defects, thus possibly producing different responses to both TID and annealing. In order to predict the correct radiation response, it is thus necessary to know the activation energy of the different trapping/de-trapping mechanisms. This information can be obtained using the isochronal annealing technique [140] for the extraction of the activation energies. For example, this allowed to correctly forecast the evolution of the leakage current in nMOS transistors in [139] and [141].

As shown in Fig. 14, the STI oxide fully surrounds and separates transistors from each other. Hole trapping in the surrounding oxide can lead to the inversion of lightly p-

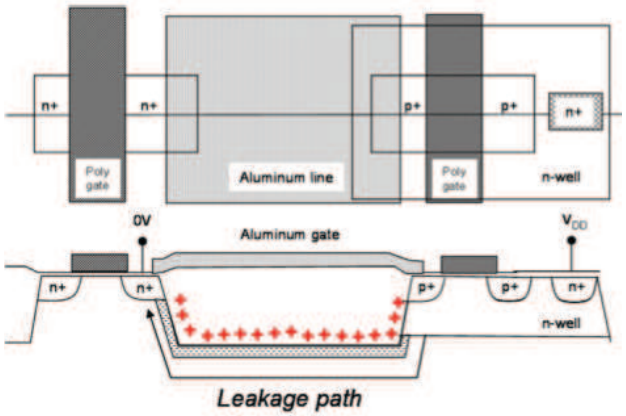


Fig. 19. Hole trapping in the STI oxide can also lead to the formation of an inversion layer in lightly-doped p regions under the STI, where leakage currents can flow between n-doped regions that should instead be fully isolated (inter-device leakage). Here, the case of a path between a drain/source and an n-well is shown in an nMOSFET. In a real circuit, the aluminum (or copper) line is a metallization layer used for routing that "accidentally" overlaps the potential leakage path, generating a field in the underlying STI oxide that can influence charge yield and transport during irradiation. It acts as a "gate" of the parasitic transistor on the FOXFET. (After [67].)

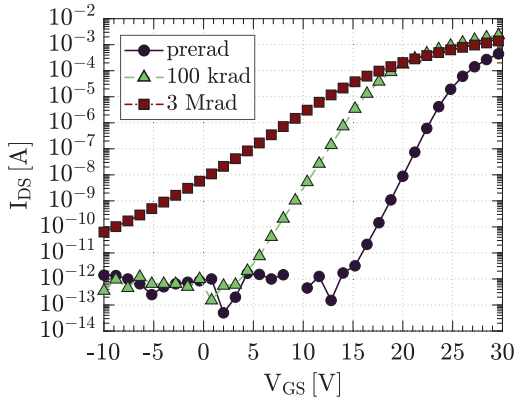


Fig. 20. Transfer characteristic of the FOXFET using two n-wells at minimum distance as source and drain electrodes, and a polysilicon line over the STI as gate in a 130-nm technology. During irradiation, the gate was kept at V_{dd}. The width of this transistor was 200 μm and V_{DS} was 1.2 V during the measurement. Before irradiation, V_{TH} of the FOXFET was around 25–30 V, significantly decreasing with TID and opening a potential leakage path even when the poly gate is kept at 0 V.

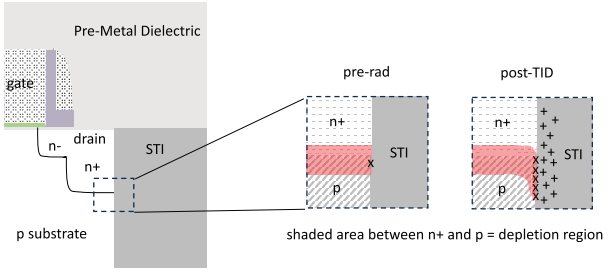


Fig. 21. Conceptual illustration of the influence of TID on the depletion region of an n+ drain diffusion in the substrate. TID-induced charge trapped in the oxide (+ symbols) influences the shape of the depletion area close to the STI. The associated increase in interface traps is represented by the larger density of the x symbols at the border between the STI and the depletion region.

doped regions under it, opening a conductive channel between n-doped regions (source or drain of nMOS transistors, n-wells) that should instead be fully isolated. These paths are schematically illustrated in Fig. 19. The evolution of these leakage currents with TID follows the same dependence on temperature and DR as the drain-source leakages since they depend on defects in the same oxide and interface. Although drain-source leakage is generally the mechanism limiting the radiation resistance of a circuit, these inter-device leakages cannot be neglected as they can contribute to the total TID-induced current consumption and disrupt specific nodes of circuits whose full isolation is fundamental for the targeted performance. The radiation response of the isolation in any CMOS technology can be measured with dedicated test structures based on Field OXide FETs (FOXFETs), see Fig. 19. An example of the characterization of the FOXFET is shown in Fig. 20, where the threshold voltage as well as the subthreshold swing change very significantly with TID.

B. Diffusion-Substrate Leakage

TID can also affect the leakage current in reverse-biased junctions like those between n or p diffusions (source/drain of a transistor) and the substrate or well where the transistor is built. This current can significantly change with TID because active interface traps located in the depletion region act as generation-recombination centers that increase the surface component of the reverse current. TID both increases their number, by depassivation related to hydrogen drift from the STI oxide, and modifies the shape of the depletion region via the electric field generated by holes trapped in the STI. This is schematically illustrated in Fig. 21 for the drain of an nMOS transistor in the substrate.

This reverse current poses a significant problem whenever, in a circuit, a floating node is used to store information. When the capacitance of the storing node is small, this leakage can lead to premature discharge and loss of information. This can be the case in dynamic random access memories (DRAMs), pixel detector arrays, and analog-to-digital converters (ADCs), where the use of sampling capacitance of large size is not possible because of area constraints. Other than by this continuous leakage current, some circuits are also affected by a leakage current fluctuation characterized by random and discrete changes of the leakage current presenting several generation rates. This gives origin to what is usually called random telegraph signal (RTS) noise and has been shown to affect CMOS image sensors (CISs), where the sense node is integrated as a floating diffusion [142], and to introduce variable retention time (VRT) in DRAMs [143]. In both cases, TID increases the RTS and the origin of the noise has been associated with a variation in the generation current at the interface of the depletion region with the STI oxide, probably due to a spontaneous structural fluctuation of complex meta-stable defects [143], [144]. These works report that the generation current is enhanced by high magnitude electric fields [electric field enhancement (EFE)], likely through tunneling mechanisms such as trap-assisted-tunneling (TAT) [145], [146], [147]. This EFE is

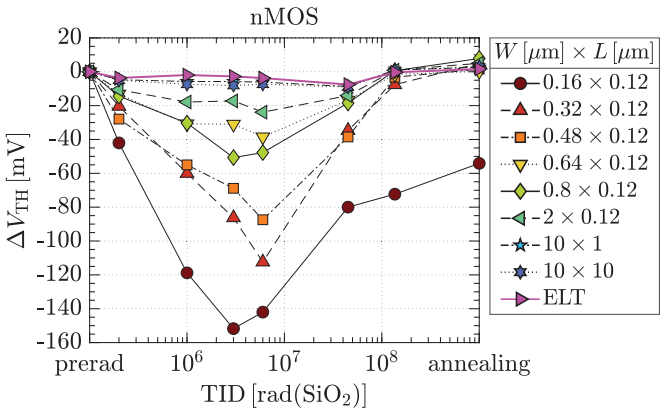


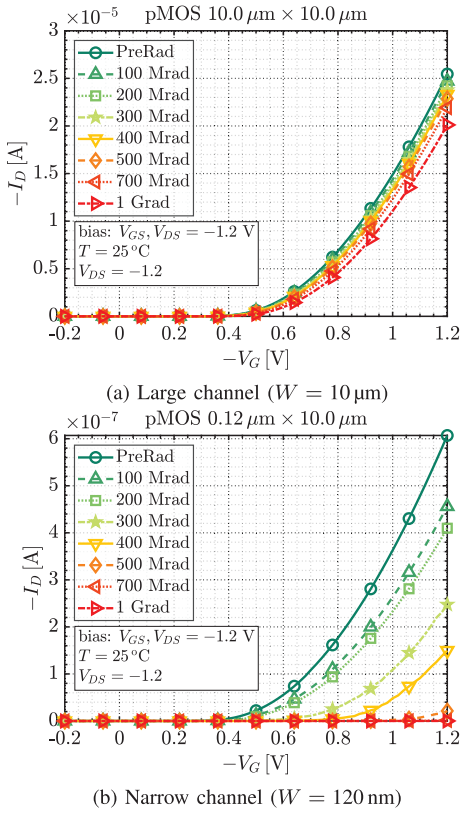
Fig. 22. Threshold voltage shift versus TID for nMOS transistors of different sizes. ELT stands for enclosed layout transistor, a ringed layout that eliminates the STI from the edge of the transistor [148], [149], [150], [151]. The last point for each series was taken after annealing for a week at 100 °C. Most transistors in the dataset were part of an array with minimum gate length (0.12 μm), and the V_{TH} shift decreases with W. The widest transistors were individual devices in the same test chip and show practically no degradation for a width of 10 μm. Their difference in L does not affect these results (After [139]).

also behind the gate induced drain leakage (GIDL) observed in MOSFETs when they are heavily turned off, a phenomenon that is also frequently reported to increase with TID.

C. Radiation Induced Narrow Channel Effect

In addition to the introduction of leakage currents, charge trapping in the STI oxide at the edge of the transistor can also affect the electrical characteristics of both nMOSFETs and pMOSFETs, altering channel parameters like the threshold voltage V_{TH}, the ON-current I_{ON}, and the transconductance. The first observation of this effect, in a 130-nm technology, was reported at IEEE Nuclear and Space Radiation Effects Conference (NSREC) in 2005 [139]. As shown in Fig. 22 for nMOS transistors, the TID-induced V_{TH} shift varies with the gate width; transistors with long and wide channel, such as the 10/10 or 10/1 μm, are almost unaffected, while in the array with the same L (0.12 μm), the V_{TH} shift increases significantly for the narrower devices. This effect was named radiation induced narrow channel effect (RINCE). The "rebound" in the evolution of V_{TH} resembles the one observed for the drain-source leakage in Fig. 15, suggesting a similar origin for the two effects. Moreover, eliminating the STI oxide at the edge of the channel with an enclosed layout transistor (ELT) design, where the drain is fully surrounded by the thin gate oxide, completely removes the V_{TH} shift, confirming the physical location of the RINCE defects in the STI at the edge of the transistor [148], [149], [150], [151].

Since that 2005 work, RINCE has been observed in all planar technologies, strongly affecting the TID response of narrow channel transistors—with the pMOSFETs exhibiting the worst degradation. As an example, Fig. 23 compares the evolution with TID of the transfer characteristics for long-channel transistors in a 65-nm technology. The maximum current that the transistor can carry when $V_{GS} = V_{DS} = V_{dd}$ (last point for each curve, at $V_{GS} = 1.2$ V), denoted by



(a) Large channel ($W = 10\,\mu$m)

(b) Narrow channel ($W = 120$ nm)

Fig. 23. Transfer characteristics of long-channel ($L = 10\,\mu$m) pMOS transistors in a 65-nm technology irradiated up to 1 Grad(SiO$_2$). The narrow-channel device in (b) ($W = 0.12\,\mu$m) has a remarkably larger performance degradation than the wide-channel one in (a) ($W = 10\,\mu$m).

I_{ON}^{sat}, only marginally decreases for the large-channel transistor, while it collapses at high doses for the narrow-channel one. This is illustrated in Fig. 24 for both 65 and 28-nm samples; the percentage degradation of I_{ON}^{sat} in pMOSFETs considerably increases for narrower channels, while for nMOSFETs, there is a more significant "rebound."

As illustrated in [152], it is the trapping of charges in the shallower region of the STI sidewall that determines the TID evolution of the channel's parameters. This superficial region is crossed by the field lines generated by the gate voltage, leading to both hole trapping in the oxide and depassivation of interface states at the oxide-channel border—the latter requiring field-driven hydrogen ions' drift. The electric field resulting from the build-up of a charge layer in the STI oxide and at its interface determines a change in the charge balance in the silicon body close to the STI. This interferes with the field generated by the gate voltage, rendering the surface potential in the region around the STI corner more (or less, depending on the polarity of the charge in the traps and the channel) easily controllable by V_{GS}.

In pMOS transistors, positive charge (holes) is trapped in both the STI oxide and at its interface and originates an electric field that drives the n-doped body of the pMOSFET toward accumulation. The gate voltage thus progressively loses some control on the channel region close to the STI sidewalls as TID accumulates. In nMOS transistors, as already shown in Section III-A for the leakage current, the different

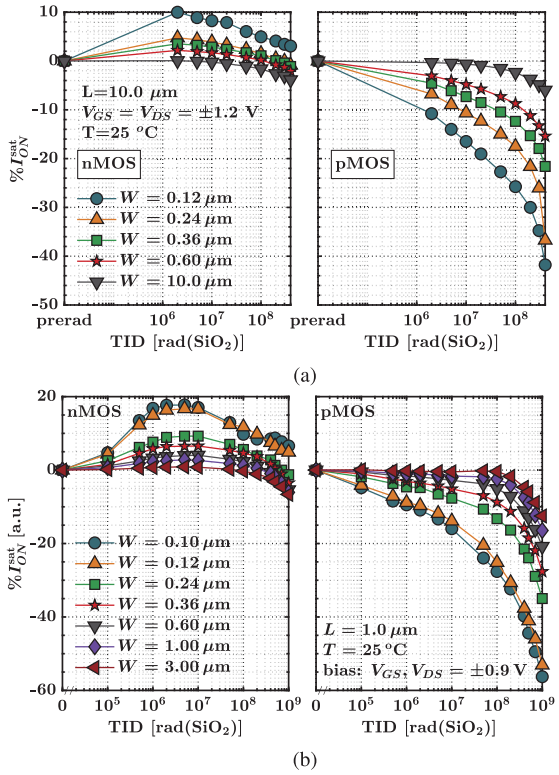


Fig. 24. Evidence of RINCE in (a) 65- and (b) 28-nm technologies. Long-channel transistors (L = 10 μm) with smaller width experience a stronger variation in their maximum driving strength (I_{ON}^{sat}) with irradiation in both technologies and for both polarities.

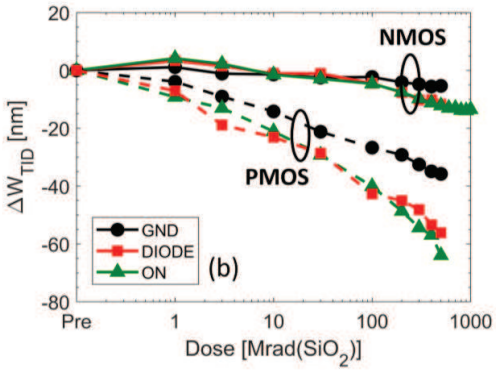


Fig. 25. Modification of the effective channel width as a function of TID in 28-nm transistors. Three different bias conditions were used in this study for both nMOS and pMOS transistors: GND for all terminals grounded, ON for $V_{GS} = V_{dd}$ and all other terminals grounded, and DIODE for $V_{GS} = V_{DS} = V_{dd}$. In the absence of V_{GS}, the effect is reduced by the smaller field-driven hydrogen ions' drift that leads to a lower activation of interface traps. (After [152].)

dynamic evolution of oxide and interface traps explains the "rebound" evident in Figs. 22 and 24. In terms of drain current, the effect of the charge trapped in the STI can be represented by a simplified model where it modulates the effective channel width. This model was used in [152] to extract, from experimental data on a 28-nm technology, the TID-induced change in channel width of transistors of both polarities. The result in Fig. 25 shows how, in pMOS transistors, the effective channel width can be reduced by more

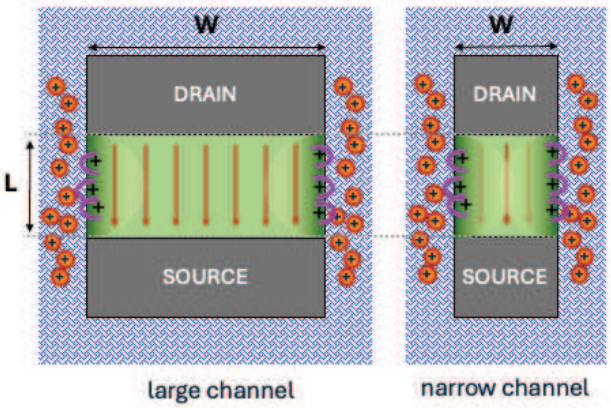


Fig. 26. Schematic of the RINCE in pMOS transistors seen from above (layout view). The textured STI oxide fully surrounds the FETs, where the current is represented by the arrows in the channel. Charges trapped in both the STI oxide (yellow circles) and in interface traps (horseshoe-shaped purple lines) are holes. The channel region influenced by the electric field generated by the trapped charge is represented by the darker green halos at the edge of the transistors. This region is only a small fraction of the channel in wide transistors (left) but extends to the whole channel for narrow ones (right).

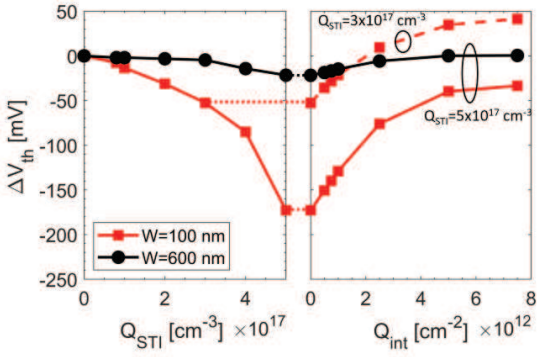


Fig. 27. Evolution of the threshold voltage with TID of nMOS transistors in the 28-nm technology with L = 1 μm, extracted from I_D-V_{GS} TCAD simulations. To the left, only positive charge in the STI is added to simulate TID-induced hole trapping (Q_{STI}). Then, for two unchanged values of Q_{STI}, an increasing density of interface traps is added. Only the narrow-channel transistor shows a considerable effect of the charge trapped in the STI sidewall on the channel properties. This clearly illustrates the origin of RINCE. (After [152].)

than 60 nm at ultra-high doses. In narrow channel transistors, this is a very considerable change, but its impact becomes less significant in large-W devices, where most of the channel is too far from the STI to feel the influence of trapped charge. This difference between narrow and wide transistors, which is schematically represented in Fig. 26, was reproduced with TCAD simulations where charge trapping in the STI and at its interface was added [152]. The V_{TH} evolution with TID reported in Fig. 27 shows that the same amount of charge in the STI sidewall that originates the "reboud" of V_{TH} in the narrow-channel transistor has an insignificant impact on the V_{TH} of the large-channel one.

D. Influence of the Body Doping and Halo Implantation

The relevance of the effect of charge trapping in the STI on the transistor's characteristics is determined by the doping

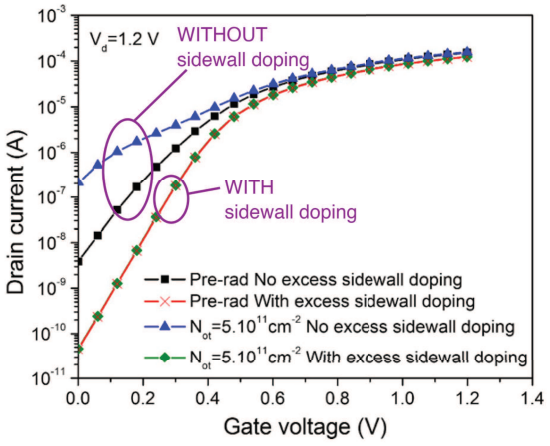


Fig. 28. Pre- and post-irradiation simulated transfer characteristics of planar MOSFET transistors with drain-source voltage $V_d = 1.2$ V before and after the addition of positive fixed charge in STI with density of $N_{ot} = 5 \times 10^{11}$ cm^{-2}. Transistors with excess sidewall doping of 5×10^{18} cm^{-3} do not show any change (green and red curves overlap), while in transistors without this doping, a considerable increase in sub-threshold current appears. (After [154].)

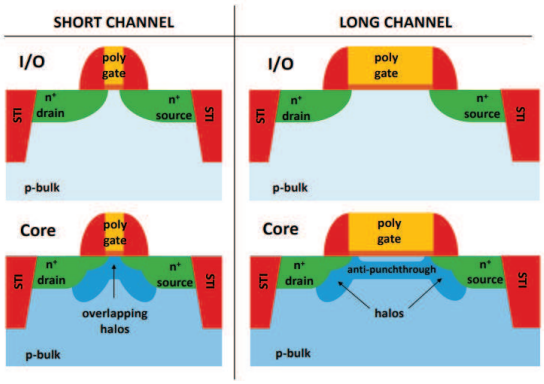


Fig. 29. Schematic of generic I/O and core nMOSFETs designed with short and long-channel dimensions. Core transistors are typically fabricated by using LDD extensions, anti-punchthrough, and source/drain halos. Dark blue used for the anti-punchthrough and halo regions represents a higher doping with respect to the substrate. While in long-channel transistors, the source and drain halos are separate, in short-channel devices, the halos overlap and increase the effective doping of the whole channel. (After [86].)

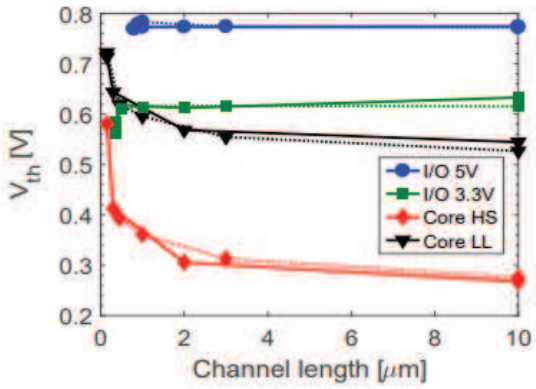


Fig. 30. Threshold voltage V_{TH} as a function of the channel length for fresh nMOSFETs fabricated with a 150-nm planar MOSFET technology. Continuous lines refer to transistors with $W = 0.8$ μm (I/O transistors) and $W = 0.3$ μm (core transistors—HS: high speed and LL: low leakage). Dotted lines refer to transistors with $W = 10$ μm. In I/O devices, without halo implants, V_{TH} decreases in very short channel transistors. Conversely, the trend of $V_{TH} - L$ of core devices is strongly characterized by the RSCE, indicating that highly doped halo implantation effectively increases overall channel doping. (After [86].)

levels in the body of the device (bulk or well), close to the STI borders. This has been studied both with analytical methods and simulations [136], [153], [154], [155]. The high variability of the TID-induced drain-source leakage current in nMOS transistors has been shown to originate from the statistical variation of the doping implantation process in the regions close to the STI [154]. In particular, a study [153] showed through simulations that the radiation-induced leakage current decreases in 90-nm nMOSFETs when the doping along the STI sidewalls is increased. Similar results were also obtained in recent works [154], [155] where radiation-induced STI effects were modeled as a function of the doping implants in the bulk. Fig. 28 shows the influence of an excess sidewall doping on the subthreshold regions of simulated nMOSFETs [154]. The I_D-V_{GS} curves evidence the high TID-tolerance of the transistors with 5×10^{18} cm^{-3} of excess doping, as the electrical field generated by the positive trapped charge in the STI is not able to invert the body at the edge of the transistor. All these results indicated that any manufacturing step affecting the effective body doping of the transistor also influences its TID response.

In scaled-down CMOS technologies, some processing steps introduced specifically to moderate short-channel effects alter the native body doping along the STI sidewall. These are the anti-punchthrough and halo implantation schematically illustrated in Fig. 29 that increase the body doping and influence the TID response [86], [156]. While the anti-punchtrough is implanted in the channel area a few nanometers under the gate oxide, the halos are implanted in the body at low energy and large incident angle to allow the implanted dopants to penetrate underneath the edge of the spacers and of the gate stack. Increasing the body doping at the channel periphery of the drain and source, halos prevent the loss of L_{eff} by attenuating the expansion of the drain/source depletion regions into the channel area [157], [158]. In short-channel transistors, the drain and source halo implantation regions overlap [159], [160], causing an increase in the doping in the whole channel that directly influences (increases) the threshold voltage of short-channel transistors [159], [160], [161]. This increase of V_{TH} in short-channel transistors is called "reverse short-channel effect (RSCE)" [86], [160], [161] and is typical of scaled CMOS technologies with aggressive halo doping concentration. An example is shown in Fig. 30 for transistors built in a 150-nm planar MOSFET technology.

Because of the larger channel doping in short transistors [halo overap and radiation-induced short channel effect (RISCE)], these devices are less sensitive to TID [86], [91], [94], [118], [161]. Fig. 31 reports the representative example of a 28-nm technology irradiated up to ultra-high doses [161]; transistors with narrow channel ($W = 100$ nm) exhibit a much larger degradation when their channel length is larger. This halo-related effect is only visible in narrow transistors, i.e.,

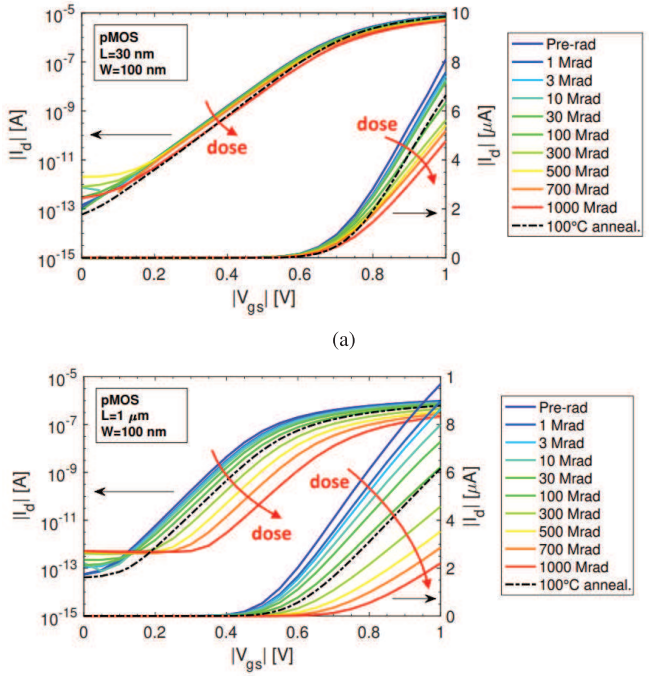


Fig. 31. Degradation of I_D-V_{GS} in the linear region (V_{DS} = −0.1 V) of narrow pMOSFETs with W = 100 nm. Transistors were irradiated at room temperature up to 1 Grad(SiO_2) and then annealed for 24 h at 100 C. The bias during irradiation and annealing was $V_{GS} = V_{DS}$ = −0.9 V. (After [161].) (a) Short channel, L = 30 nm. (b) Long channel, L = 1 μm.

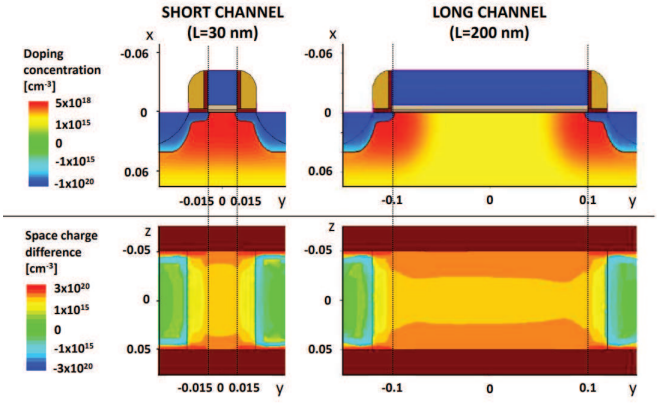


Fig. 32. 3D TCAD simulations of a narrow-channel 28-nm pMOSFETs. At the top, a vertical cut-plane shows the doping concentrations in short (left) and long (right) channel transistors (halo in red). At the bottom, a horizontal cut plane at 2 nm below the gate oxide/Si interface shows the difference in the space charge density between pre-rad and irradiated devices in short and long channel pMOSFETs. (After [161].)

when the TID degradation is dominated by the charge trapping in the STI (RINCE) and was clearly demonstrated in 3D TCAD Sentaurus simulations for a 28-nm technology [161]. Fig. 32 shows the simulated 3D structure of a pMOSFET with L = 200 nm. The side view at the top shows the doping concentration in the short and long channel pMOSFETs: the highly doped regions in red identify the halo implants, which almost overlap each other in the short channel transistor with L = 30 nm. The top view of the transistor on the bottom refers

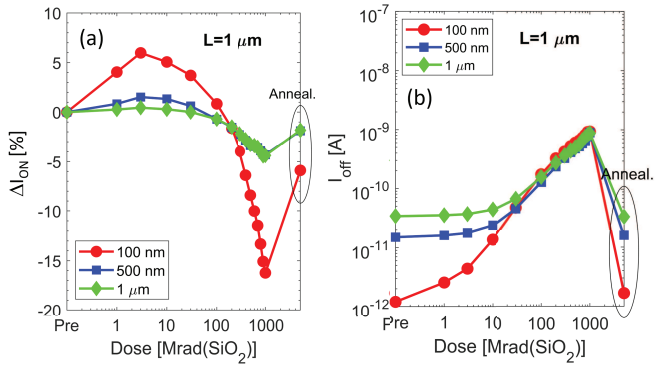


Fig. 33. Comparative evolution with TID of (a) maximum drive current (I_{ON}) and (b) leakage current (I_{OFF}) in nMOS transistors with L = 1 μm and channel width of 200 nm, 500 nm, and 1 μm in 28-nm technology. Irradiation and 24 h annealing at 100 °C took place with V_{GS} = 1 V and all other terminals grounded. The pre-rad leakage value is different before irradiation because I_{OFF} is the current flowing at V_{GS} = 0 V and $V_{DS} = V_{dd}$, a condition where the transistors are already in weak inversion; thus, the current depends on the W/L ratio. At high TID levels, instead, leakage flows in the lateral parasitic transistors and only depends on L, which is the same for the three plotted devices. (After [152].)

to a horizontal cut plane at x = 0.002 μm, which is 2 nm below the gate Si/SiO_2 interface. The transistors were simulated in the "ON" condition, i.e., in linear region with $|V_{DS}|$ = 0.1 V and $|V_{GS}|$ = 1 V. The plots report the difference in the space charge density between a fresh and an irradiated device. TID was simulated by inserting a uniform volumetric density of positive charges $Q_{STI} = 3 \times 10^{18}$ cm^{-3} in the STI, equal to 8×10^{12} cm^{-2} along the STI sidewalls, levels in agreement with previous works [136]. In both the short and long channel cases, the space charge density is little affected by TID (yellow area) close to the source and drain diffusions, which is due to the presence of the halos. However, in the short-channel transistor, the difference in the space charge density is smaller everywhere, evidencing how the higher body doping from the halos reaches the full channel and determines a decreased sensitivity to the charge trapped in the STI.

The modulation of RINCE introduced by the halos concerns both pMOS and nMOS transistors and has also been observed in FinFET technologies [94], [118]. However, similar to most TID-induced effects, its observability is strongly dependent on the details of the manufacturing process and on the type of transistor (I/O, core, low-leakage, high-speed, low-V_{TH}, and so on).

E. Importance of the Depth of Trapping in the STI

Both drain-source leakage and RINCE originate in the STI at the edge of the transistor (sidewall) and are influenced by the body doping; however, the mechanisms responsible for these phenomena take place at different depths in the STI oxide [91]. This was demonstrated in a recent work [152] based on the observation that in nMOS transistors from many planar technologies in the range from 65 to 28-nm, the evolution with TID of the channel parameters (I_{ON}, V_{TH}, and g_m) and the leakage current is strongly dissimilar. Fig. 33 illustrates this difference for long-channel nMOS transistors in a 28-nm technology. The maximum drive current I_{ON}

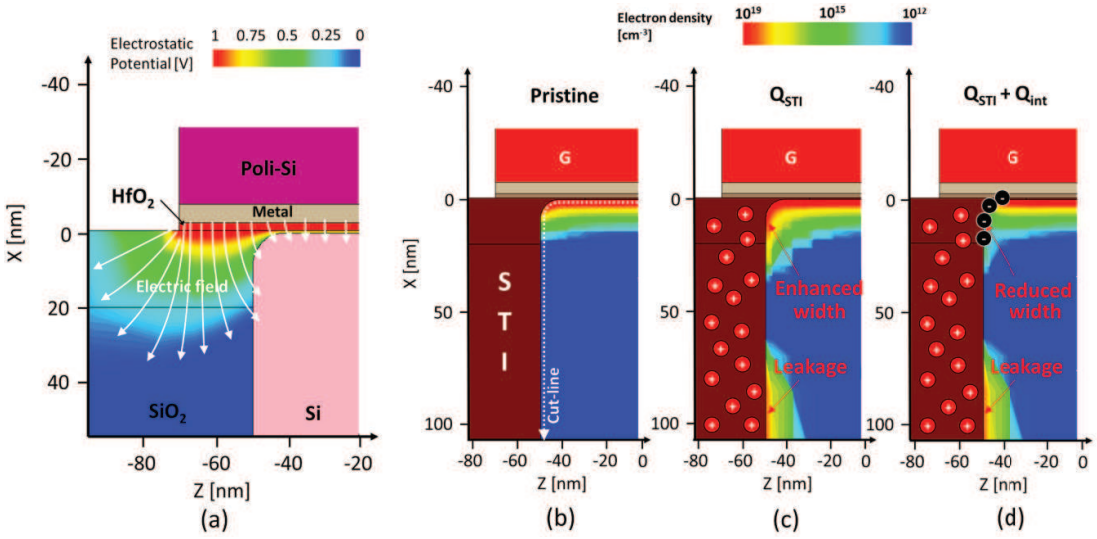


Fig. 34. TCAD simulation of a 100/200 nm nMOS transistor in 28-nm. The cut view shows only half of the transistor, the origin along the Z-axis being at the center of the channel width. The cut is in the middle of the channel length (Y-axis, not shown, which is orthogonal to the page). (a) Intensity and direction of the electric field in the oxides for V_{GS} = 1 V, which corresponds to the ON-bias condition during irradiation. (b)–(d) TID-induced mechanisms influencing the channel parameters (I_{ON}, V_{TH}, and transconductance, respectively) while increasing I_{OFF}. In this case, the color scale indicates the electron density in the Si channel when V_{GS} = 1 V (channel ON). (b) Pre-irradiation without TID-induced trapped charge in the oxides, (c) at high doses with holes trapped in the STI ($Q_{STI} = 5 \times 10^{17}$ cm^{-3}), and (d) at ultra-high doses with trapping of both positive charge (holes in the oxide, $Q_{STI} = 5 \times 10^{17}$ cm^{-3}) and negative charge (electrons in interface traps, $Q_{int} = 7.5 \times 10^{12}$ cm^{-3}). Q_{STI} is uniformly distributed in the STI, while Q_{int} is localized at the Si/SiO$_2$ interface close to the upper corner of the STI, as shown in (d). (After [152].)

shows the W-dependent "rebound" typical of RINCE, while the leakage current converges to the same continuous increase with TID for all widths. Not shown in the figure, the results for transistors with different biases during exposure evidenced that only the variation of parameters related to the channel was influenced by the applied gate voltage, while the TID evolution of I_{OFF} was the same for all bias conditions. All these results suggested that the charge trapping mechanism responsible for the leakage takes place in a region beyond the reach of the electric field generated by V_{GS}, likely in a deeper portion of the STI sidewall. This model was confirmed by 3D TCAD simulations yielding results such as the one shown in Fig. 34 for a narrow nMOSFET. While hole trapping takes place in the whole of the sidewall STI oxide [Q_{STI} in Fig. 34(c)], interface traps are depassivated only in its shallower portion leading to electron trapping [Q_{int} in Fig. 34(d)]. This is due to the fact that hydrogen ions' drift, responsible for the activation of interface traps, is driven by the electric field from the gate electrode that only extends to the superficial region of the STI, as shown in Fig. 34(a). On the contrary, the deep leakage path that opens when sufficient holes are trapped in the STI in Fig. 34(c) and (d) extends as long as a net increase in hole trapping takes place due to the lack of sufficient in-depth interface trap depassivation. The drain-source leakage current is the same for each of the two sidewalls, thus independent of the channel width (see the right chart in Fig. 33) but directly proportional to its length. These results refer to 28-nm transistors where an anti-punch-through implant is situated at a depth of about 50 nm below the gate oxide and illustrate the importance of this implant to "separate" the superficial channel from the in-depth parasitic leakage channel. The characteristics of the implant could thus, in principle, be used to reduce or even potentially eliminate the radiation-induced leakage.

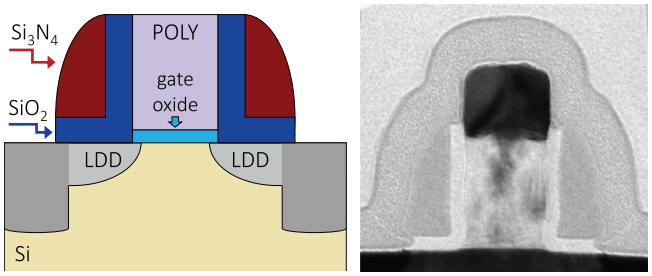


Fig. 35. (a) Schematic of spacer insulator that is made of a first layer of SiO$_2$ (in blue) and then a thicker layer of Si$_3$N$_4$(in purple). (b) TEM image of a transistor where the two layers composing the spacers are well visible.

IV. Spacers

Sidewall spacers are thick oxides placed alongside the poly-silicon/metal gate, as shown schematically in Fig. 35(a) and depicted by the TEM image in Fig. 35(b). They typically consist of a tens of nanometers thick layer of silicon nitride (Si$_3$N$_4$) separated from the polysilicon gate and the source/drain diffusions by a thinner but still relatively thick layer of SiO$_2$. Spacer oxides are necessary during the manufacturing process to create LDD diffusions on the side of the conductive channel [162]. LDD diffusions play a key role in deep sub-micrometer nodes by reducing hot-carrier effects [163]. Despite not being in direct contact with the conductive channel, spacers have been identified as responsible for RISCEs, a group of TID-induced mechanisms characterized

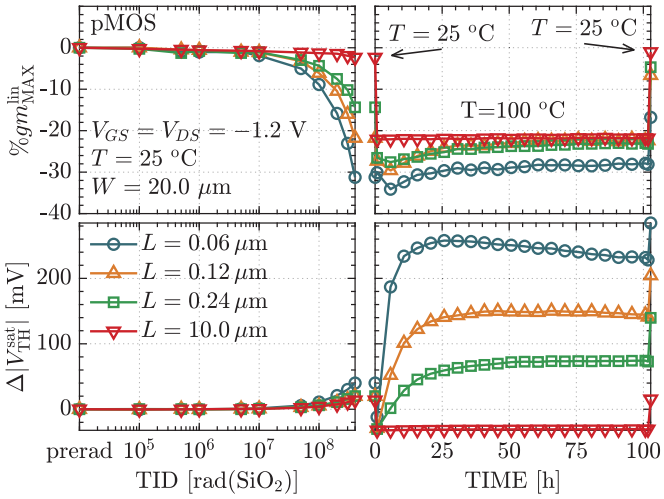


Fig. 36. Percentage variation of the maximum of the transconductance measured in linear region (gm_{MAX}^{lin}, top row) and threshold voltage shift (bottom row) for pMOS transistors with $W = 20$ μm and different channel lengths. The transistors, from a 65-nm CMOS technology, were measured during irradiation at ~10 Mrad(SiO$_2$)/h (left column) and $T = 100$ °C annealing (right column). The first and the last point of the annealing were taken at $T = 25$ °C, while all other measurements were performed at $T = 100$ °C. Both during irradiation and annealing, the devices were kept in the diode configuration ($V_{GS} = V_{DS} = -1.2$ V). (After [166].)

by greater degradation in short channel transistors. While first introduced in [164], the best description of RISCE can be found in [141], [165], and [166]. RISCE has been observed in 180-nm [167], 130-nm [164], [168], 65-nm [141], [165], [168], and, as reported in this article, 40-nm CMOS technologies.

Fig. 36 illustrates the radiation response of pMOS transistors in a 65-nm CMOS technology susceptible to RISCE. The top row of the plot shows the percentage variation of the maximum of the transconductance measured in the linear region (gm_{MAX}^{lin}) during irradiation and annealing, while the bottom row displays the threshold voltage shift. The devices have the same channel width $W = 20$ μm and different channel lengths, ranging from $L = 60$ nm to $L = 10$ μm. The choice of this large W entails the avoidance of significant narrow-channel effects from the STI oxide, as discussed in Section III-C. Moreover, the results similar to those presented in Fig. 36 were obtained in ELTs [141], [167], where the effect of the STI is removed by design. During exposure (left column), gm_{MAX}^{lin} decreases more in short channel devices, reaching a maximum degradation of ~31 % in the $L = 60$ nm device. Conversely, the threshold voltage shift is relatively small and only slightly dependent on the channel length. This behavior reverses during the annealing phase (right column), with a drastic L-dependent variation of $|V_{TH}^{sat}|$ and a recovery of the transconductance. This complex behavior has been explained with a three-step process [141], [165].

- Charge accumulation in the spacers that leads to reduced carriers in the LDD regions, resulting in increased series resistance R_{SD} and a consequent reduction in drain current and transconductance [Fig. 37(a)].
- Transport of hydrogen ions (H_+) from the spacers to the gate oxide [Fig. 37(b)].

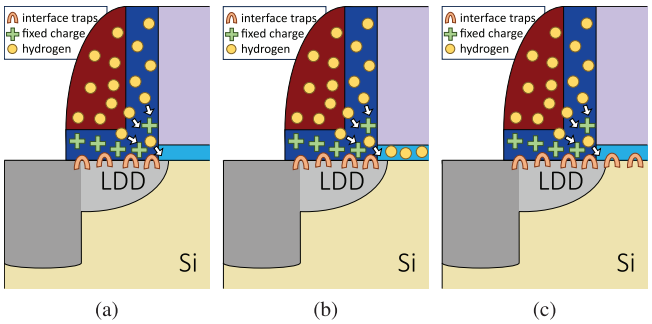


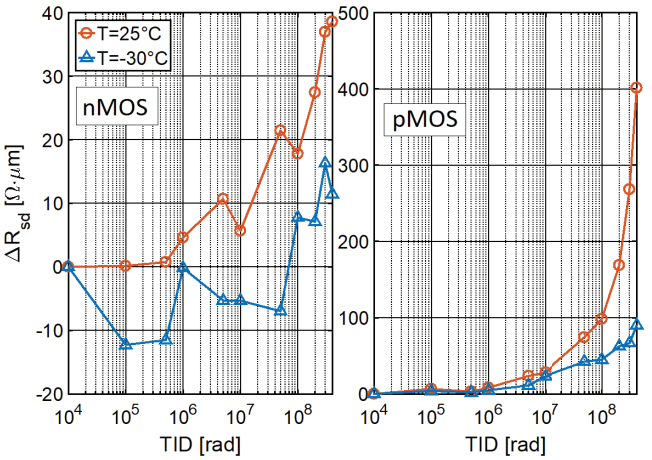
Fig. 37. Schematic of spacer-related effects. (a) Radiation-induced charge trapped in the spacers. Its presence affects the LDD extensions, increasing the series resistance. (b) H_+ (protons) drift from the spacers in the thin gate oxide. This transport is strongly dependent on temperature and electric field. (c) Hydrogen ions react at the interface causing the depassivation of interface traps. (After [141].)

- Creation of interface traps and consequent shift in the threshold voltage [Fig. 37(c)].

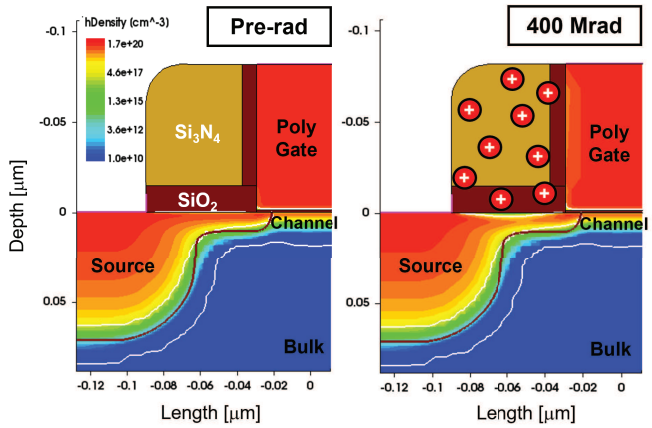
The time required for the observation of the V_{TH} shift during measurements in this 65-nm technology depends on the polarity of the transistor. At room temperature, the threshold shift is only observed after several days in pMOSFETs, while in nMOSFETs, it already appears after a few hours, suggesting a faster drift of H_+ from the spacers [141]. This makes pMOS transistors easier to study since the mechanisms in the LDD and gate oxide can be separately observed in tests conducted at $T < 30$ °C with total irradiation time below a few days. pMOS transistors have therefore been the main object of studies on RISCE and are the focus of the following discussion. However, while it is believed that the mechanisms behind RISCE in nMOSFETs and pMOSFETs are similar [141], the reason for the possible difference in H_+ transport rate in nMOSFETs and pMOSFETs remains unclear.

A. Increase in Source/Drain Series Resistance

The first observation during irradiation of pMOS transistors is a decrease in drain current and transconductance that can be attributed to an increase in the source/drain resistance in series to the channel R_{SD} [141], [165]. Fig. 38(a) shows the variation of R_{SD} for the pMOS transistors of Fig. 36 and for their equivalent nMOS transistors [141]. A single R_{SD} value is extracted for all channel lengths because, in first approximation, the source/drain series resistance is independent of L [169]. R_{SD} increases with TID, and more significantly in pMOSFETs, where it augments by ~400 $\Omega \cdot \mu$m after 400 Mrad(SiO$_2$) at $T = 25$ °C [141]. This effect in R_{SD} can be attributed to a reduction in carrier density in the LDD extensions, which is induced by the electric field generated by the charge trapped in the spacers. This is illustrated in Fig. 38(b) [165] for pMOSFETs where the charge trapped in both the spacer oxide and at its interface with the LDD region is positive [see Fig. 37(a)]. The fact that, in nMOS transistors, electrons are trapped in interface traps and compensate some of the holes trapped in the spacer oxide explains their smaller R_{SD} increase.



(a)



(b)

Fig. 38. (a) Radiation-induced increase in series resistance for nMOS and pMOS transistors exposed to 400 Mrad(SiO_2) at $T = 25$ °C and $T = -30$ °C. (b) TCAD simulation of the effects of the charge trapped in the spacers of a pMOS transistor. The charge trapped in the spacers affects the carrier concentration in the LDD extension, increasing R_{SD}. (After [141] and [165].)

Since the voltage drop across R_{SD} ($\Delta V_{R_{SD}}$) increases with source-drain current, shorter devices experience higher $\Delta V_{R_{SD}}$ for the same amount of charge trapped in the spacers (and thus for the same increase in series resistance), as illustrated by the following equation:

$$\Delta V_{R_{SD}} = R_{SD} \times I_{DS} = \frac{r_{SD}}{W} \times \frac{W}{L} i_{DS} = \frac{r_{SD} \times i_{DS}}{L} \qquad (5)$$

where r_{SD} is R_{SD} normalized by W and i_{DS} is the current of the device normalized to its dimensions. In fact, in first approximation, R_{SD} decreases linearly with W, making the voltage drop on R_{SD} roughly independent of W. From (5), it clearly appears that, for the same increase in series resistance, shorter channel transistors experience a larger drain-source voltage drop $\Delta V_{R_{SD}}$ because of their larger current. In physical terms, therefore, this is not a real "short-channel effect" since the series resistance increase does not depend on L (or on W) although it manifests as such in parametric evolution with TID—as for the gm_{MAX}^{lin} in Fig. 36.

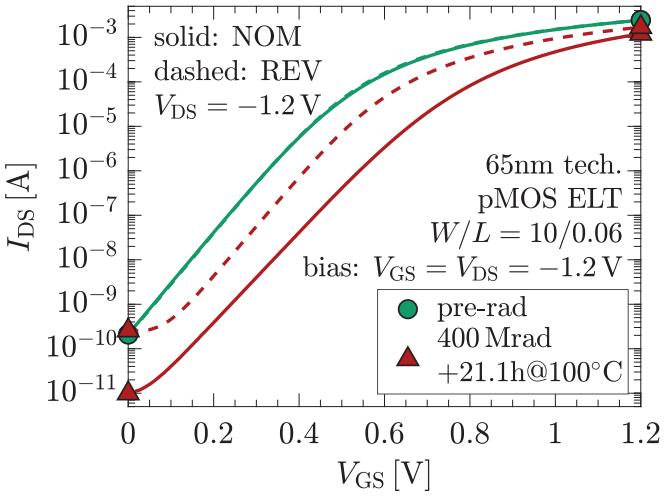


Fig. 39. I_D-V_{GS} characteristics of a $L = 60$ nm and $W = 10$ μm ELT pMOSFET irradiated to 400 Mrad(SiO_2) and then annealed for ~21 h at 100 °C. The device was biased in the diode configuration ($V_{GS} = V_{DS} = -1.2$ V) during both irradiation and annealing. Solid lines report the current in the nominal configuration, and dashed lines display the drain current in the reversed configuration [141], [166]. The measurements were performed in the saturation region ($V_{DS} = -1.2$ V). (After [141].)

B. Threshold Voltage Shift

The hydrogen ions released by radiation in the spacers can drift to the gate oxide [Fig. 37(b)] and generate interface traps by depassivating dangling bonds [Fig. 37(c)]. Charge trapped at the interface can shift the threshold voltage by changing the potential barrier in the channel.

Post-irradiation tests at different biases revealed the strong sensitivity of this effect to voltage [141]. In particular, $|V_{GS}| > 0$ V has been found to significantly accelerate the transport of H_+ from the spacers into the gate oxide. Another distinctive bias-dependent effect of RISCE is to make the transistors asymmetric, meaning that the I_{DS} current changes when the source and drain terminals are reversed. In other words, the behavior of the device depends on which terminal is used as the source and which terminal is used as the drain. The TID-induced asymmetry arises when $|V_{DS}| > 0$ V is applied during irradiation and annealing. The source-to-drain voltage promotes the transport of H_+ and the consequent formation of interface traps on one of the two sides of the transistor, making the potential barrier variation somewhat localized close to either the source or drain side, depending on the type of the transistor [141], [165], [166]. Another potential explanation for the radiation-induced asymmetry is the difference in charge yield on the two sides of the device, caused by different biases applied [170]. The difference in threshold voltage shift between nominal configuration (i.e., measured using the same roles for source and drain as those employed during irradiation and annealing) and reversed configuration is clearly illustrated in Fig. 39, where the $I_D - V_G$ characteristics of a $L = 60$ nm ELT pMOS transistor irradiated to 400 Mrad(SiO_2) and then annealed for ~21 h at 100 °C are reported [141], [166]. In this figure, the solid lines represent the drain current measured in the nominal configuration (NOM), while the dashed lines represent the drain current in the reverse configuration (REV).

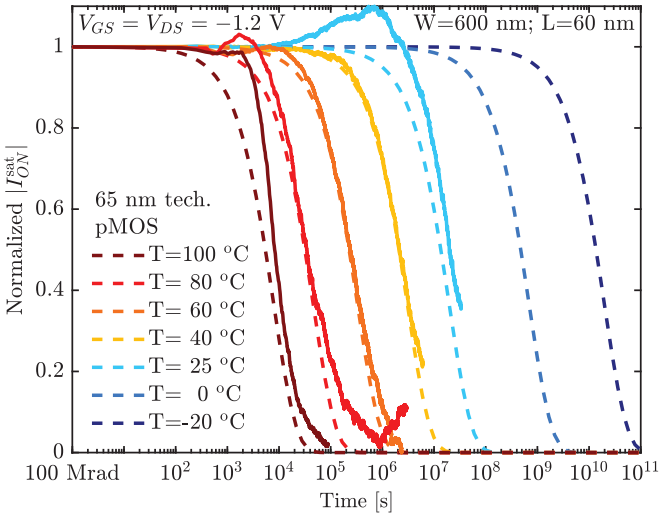


Fig. 40. Solid lines: normalized I_{ON}^{sat} of pMOSFET in 65-nm technology irradiated to 100 Mrad(SiO_2) and subsequently annealed at different temperatures. Dashed lines: prediction of the evolution based on the activation energy extracted from the data at 100 °C, 80 °C, 60 °C, and 40 °C. The $T = 25$ °C measure was used to confirm the validity of the model. (After [141].)

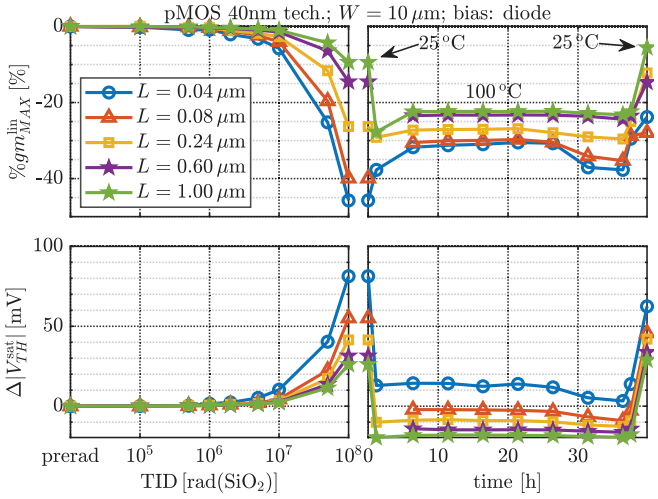


Fig. 41. RISCE in 40-nm CMOS technology. Short devices show a larger degradation in this process. However, differently to 130- and 65-nm nodes, a large V_{TH} shift is measured already during room temperature irradiation.

Prior to irradiation, the device is symmetric, meaning that changing the role of source and drain does not change the I_D-V_{GS} characteristic (green lines). At the end of the test, the device is clearly asymmetric, with a much larger V_{TH} shift measured in the nominal configuration.

The formation of interface traps on one of the sides of the device when irradiated with a $|V_{DS}| > 0$ V was also confirmed by charge pumping measurements [141], [165].

As previously mentioned, the rate of transport of hydrogen ions from the spacers to the gate oxide is temperature dependent. The solid lines in Fig. 40 show the evolution in time of the normalized I_{ON}^{sat}. The devices have been irradiated to 100 Mrad(SiO_2) at $T = 25$ °C and then annealed at different temperatures. The devices were biased in the diode configuration ($V_{GS} = V_{DS} = -1.2$ V) during both irradiation and annealing. The use of I_{ON}^{sat} instead of V_{TH} is justified by the fact that V_{TH} shift is the dominant degradation mechanism during annealing (Fig. 36). Using the data at 100 °C, 80 °C, 60 °C, and 40 °C and the approach proposed by Schwank et al. [21], the activation energy of the ΔV_{TH} shift process was estimated to be $E_A \simeq 0.92$ eV, a value close to H_+ transport in SiO_2 films [14], [171], [172]. Using the activation energy, it is possible to predict the evolution of the I_{ON}^{sat} at any given temperature, as displayed by the dashed lines in Fig. 40. The measure at $T = 25$ °C was not used to extract E_A but to confirm the validity of the model. This very important result not only helps to understand the mechanism of post-irradiation degradation but also provides practical insights. A chip kept at −30 °C (as those in the inner layers of particle detectors at the HL-LHC) should function without any significant degradation of I_{ON}^{sat} for at least 200 years. This means that, for applications where chips are maintained at low temperatures, the typical 100 °C annealing required in many qualification procedures (see [173]) can greatly overestimate device degradation.

C. RISCE in Other CMOS Technologies

RISCE has been identified in several CMOS nodes and processes other than the 65-nm technology presented so far. RISCE was observed in 180-nm ELT devices [167], a 130-nm technology [164], [166], and 65-nm CMOS processes from different foundries [168]. The present work reports the presence of RISCE also in a 40-nm CMOS technology. Fig. 41 displays the percentage degradation of the transconductance and the threshold voltage shift in pMOS transistors in a 40-nm process exposed to 100 Mrad(SiO_2) and then annealed to 100 °C. The devices have the same W and different channel lengths. Different from what happens in 130- and 65-nm technologies, in this 40-nm node, the V_{TH} shift of pMOSFETs is evident already during room temperature irradiation. As for the other nodes, also these devices become asymmetric (not shown). More advanced technologies like 28- or 16-nm FinFET do not seem to be sensitive to RISCE [91], [94], [161], [174], [175]. However, the impact of spacer design in the radiation response of 14-nm silicon-on-insulator (SOI) FinFETs technology has been evaluated, demonstrating its impact even in this advanced node [176].

V. ELDRS in CMOS

Although bipolar transistors are known to suffer from enhanced low-DR sensitivity (ELDRS) [177], CMOS technology is generally considered insensitive to true dose-rate effects [71], [173], [178], [179]. The origin of this difference lies in the different characteristics of the oxides that determine the radiation response of these devices. The oxides responsible for the TID sensitivity of bipolar transistors are thick, rich in defects, and crossed by low electric fields. On the other hand, the primary source of the TID-induced performance degradation in MOS transistors from older nodes is the thin, high-quality gate oxide, which is typically crossed by relatively high electric fields [173], [178]. However, as seen above, the radiation response of modern CMOS technologies is primarily affected by the charge trapped in auxiliary

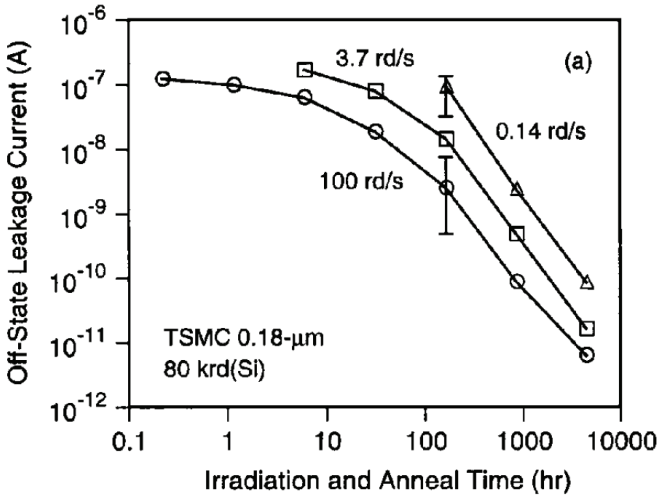


Fig. 42. ELDRS in a 180-nm CMOS technology. For a given irradiation and annealing time, the leakage current is higher in transistors irradiated at a lower DRs. (After [180].)

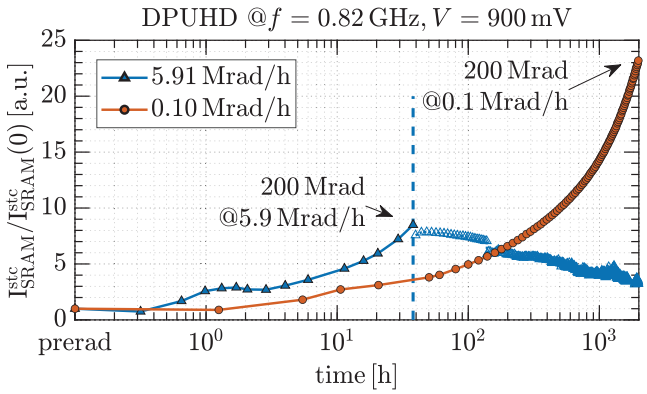


Fig. 43. Static current increase in SRAMs in 28-nm technology exposed to 200 Mrad(SiO_2) at different DRs. The increase is larger in the device exposed at LDR, suggesting a true DR sensitivity in the opening of source-to-drain parasitic paths along the STI sidewall. (After [181].)

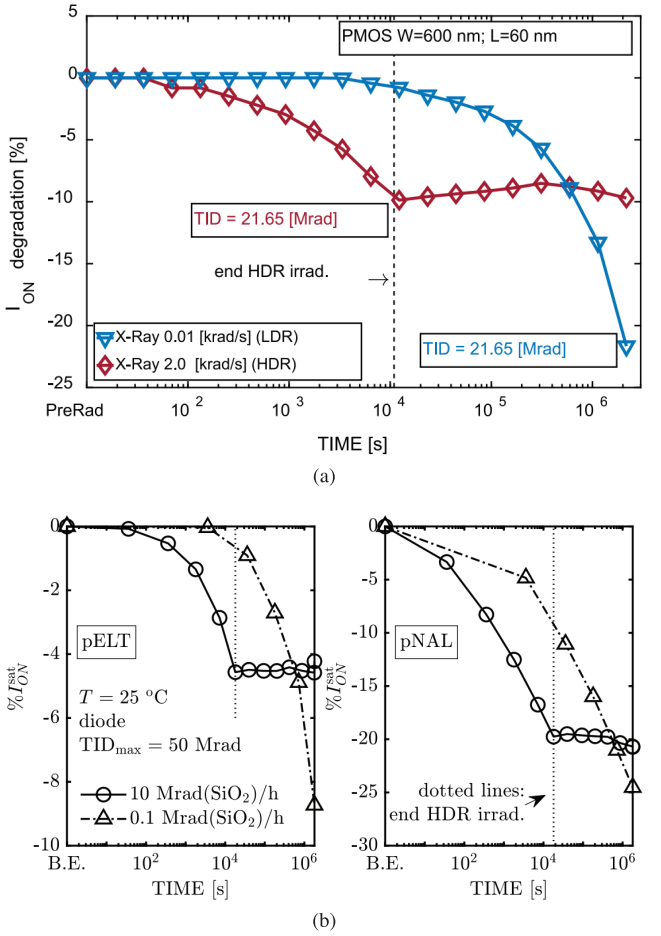


Fig. 44. (a) High DR versus LDR test for W/L = 600/60 nm pMOS transistors in 65-nm CMOS technology. For the same TID = 21.65 Mrad(SiO_2) and the same time, the percentage degradation of I_{ON} is more than twice in the LDR test. In this short and relatively narrow device, both STI and spacer oxides might be responsible for the ELDRS. (b) Actual source of the DR sensitivity is the spacer oxides. The channel in ELTs (left plot) is isolated from the STI; therefore, only the spacer can have an effect on the ON current. On the other hand, in narrow and long devices (right plot), the radiation response is dominated by the STI. In this case, the degradation is similar in LDR and HDR tests. (After [182] and [183].)

oxides such as STI and spacers. These are thick, low-quality oxides, crossed by low-electric fields, characteristics similar to the insulators employed in linear bipolar technologies, making MOS transistors potentially vulnerable to true dose-rate effects. Over the past 20 years, several experiments have revealed true DR effects in numerous CMOS technologies, caused by both STI and spacer oxides.

Witczak et al. [180] reported an enhanced DR sensitivity of the TID-induced drain-to-source leakage current in nMOS transistors in 350, 250, and 180-nm CMOS technologies that could not be attributed to a combination of charge trapping and annealing processes. As described in Section III-A, TID-induced drain-to-source leakage current is an effect related to the presence of the STI. Fig. 42 shows a representative result from this study; for any given irradiation + annealing time, the leakage current is consistently higher in devices that were irradiated at lower DRs. In the same study, 500- and 350-nm CMOS technologies from a different manufacturer were found to have no sensitivity to DR. This suggests that the effect is highly dependent on manufacturing process characteristics.

Recently, true DR effects have been observed in a commercial 28-nm CMOS technology. Fig. 43 shows the relative increase of static current of a 28-nm SRAM irradiated to 200 Mrad(SiO_2) at ~6 Mrad/h or ~0.1 Mrad/h. To ensure a fair comparison between the two tests, the HDR irradiated SRAM was annealed for a period equal to the time required to complete the low dose-rate (LDR) test. At the end of the experiment, the static current at LDR was more than twice the maximum reached in the HDR test. This greater increase was attributed to a DR sensitivity of the source-to-drain parasitic current along the STI oxide sidewall [181].

Other than STI, spacer oxides have also been found to be responsible for ELDRS in 130- and 65-nm CMOS technologies exposed to ultra-high TID [182], [183]. Fig. 44(a) shows the percentage degradation of the maximum drain current I_{ON} for W/L = 600/60 nm pMOS transistors in 65-nm CMOS technology exposed to 21.65 Mrad(SiO_2) at 2 and 0.01 krad(SiO_2)/s [182]. At the end of the experiment, the LDR device exhibited over twice the percentage degradation

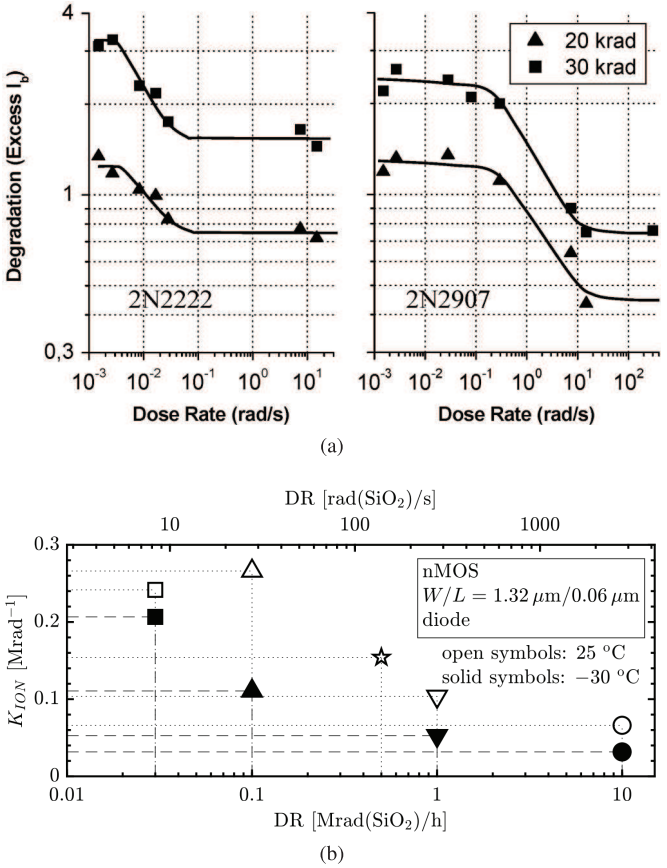


Fig. 45. Dependence on DR saturates at both high and low DRs, forming the characteristic inverted-S shaped curve. (a) Example for bipolar devices. (b) Results of MOS transistors in 65-nm CMOS technology. Note that at low temperature, the whole S-curve shifts toward lower DRs. A similar shift of the *S*-curve was predicted in [189] for bipolar devices. (After [183] and [184].)

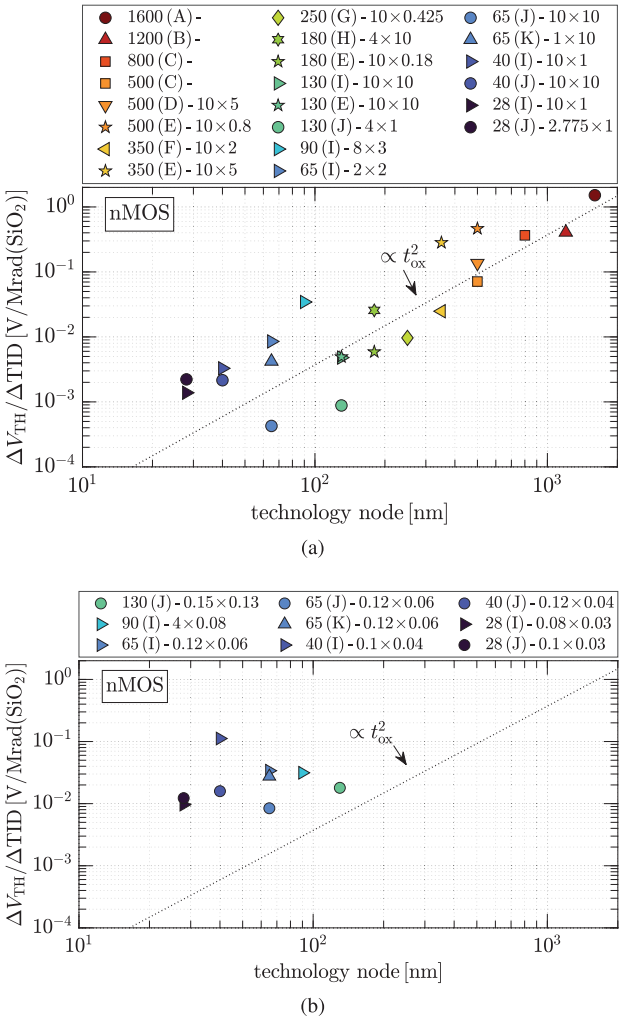


Fig. 46. Threshold voltage shift normalized to 1 Mrad(SiO_2) of TID for nMOS transistors in different technology nodes (only planar technologies). Points in (a) refer to wide and long transistors, while those in (b) refer to narrow and/or short ones in the same technologies. All measurements were taken at a TID of about 500 krad(SiO_2) at HDR to minimize the impact of interface states on ΔV_{TH}. Irradiation was performed at room temperature and with the highest electric field in the gate oxide ($V_{GS} = V_{dd}$) at an X-ray facility (40 kV field, W target). For each point, the legend indicates: the node in nanometers, the manufacturer (as a letter in parenthesis), and then the size ($W \times L$) of each transistor. The points for the four older technologies, from A to D, are from [191] and the transistor size is unknown. All other points refer to measurements performed at CERN on custom samples from commercial-grade technologies. Points below about 5×10^{-3} V/Mrad(SiO_2) correspond to measured ΔV_{TH} smaller than 3 mV at 500 krad(SiO_2) and are thus affected by a potentially large error since the extraction of V_{TH} implies an extrapolation.

observed on the sample exposed to HDR. To verify that the measured ELDRS was caused by the spacer oxides, a set of tests at ultra-high doses were carried out in [183] using ELTs with minimum channel length (L = 60 nm) that eliminate the influence of the STI. Additionally, narrow-and-long W/L = 0.12 μm/10 μm devices (NAL) were chosen to minimize the influence of the spacers and maximize that of the STI. Fig. 44(b) reports the results of a 50 Mrad(SiO_2) irradiation followed by 25 °C annealing for pMOSFETs. The ELT device exposed to LDR irradiation shows twice as much degradation as its HDR counterpart. On the other hand, NAL devices have a similar degradation regardless of the DR used.

The physical mechanisms behind ELDRS in CMOS seem to be well described by the models developed for bipolar transistors. The increase in leakage current at the LDR measured in [180] is explained by the modulating effect of space charge on the dynamics of the trapping/annealing mechanisms in the STI. In [183], measurements at different temperatures and dose-rates revealed that, for a given TID, the current degradation saturates at both high and low DRs, forming the characteristic inverted-*S* shaped curve measured in bipolar devices sensitive to ELDRS [71], [179], [180], [184], [185], [186], [187], [188], [189]. Fig. 45(a) shows an example of the inverted-*S* curve in bipolar devices [184], [190]. The results from [183] are reported in Fig. 45(b).

VI. Trends in the TID Sensitivity of CMOS Technology Nodes

A. Trend in Planar CMOS

As illustrated in Section II-B, the decrease in gate oxide thickness accompanying the down-scaling of CMOS technologies has rendered CMOS transistors less sensitive to TID effects. However, as discussed in Sections II-C and IV, the TID response is also determined, and sometimes dominated, by radiation mechanisms in the STI and spacer oxides.

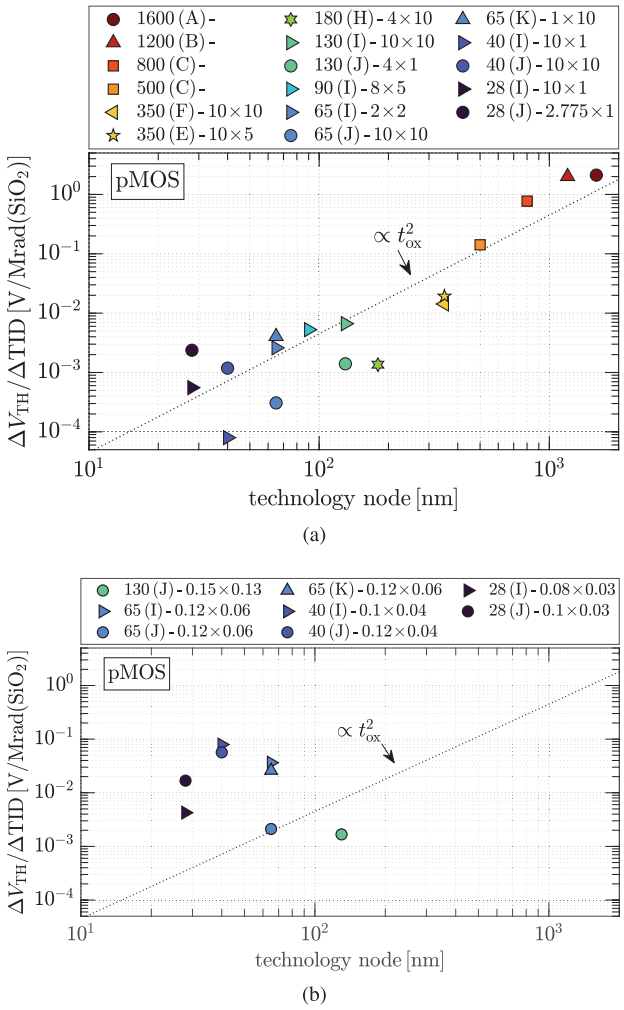


Fig. 47. Equivalent of Fig. 46 for pMOS transistors. (a) Wide and long transistors. (b) Narrow and short transistors.

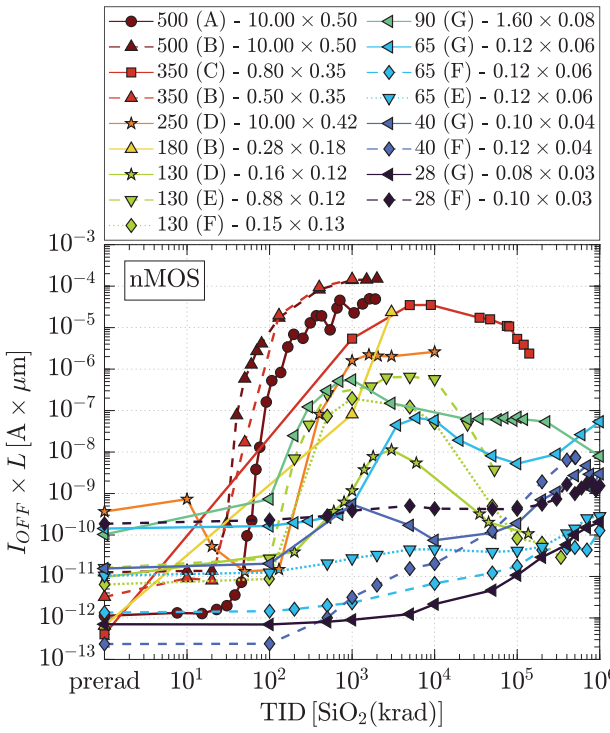


Fig. 48. Evolution with TID of the drain-source leakage current of nMOS transistors in a large number of commercial-grade planar CMOS technologies surveyed at CERN. Irradiation studies used an X-ray source (40 kV, W target) and were performed with the highest voltage applied to the gate ($V_{GS} = V_{dd}$) and all other terminals grounded. As detailed in Section II-C, the current flows at the two edges of the transistor and is thus proportional to the channel length (not the width). To make the results directly comparable, the measured I_{OFF} is normalized to the channel length (with a multiplication, since the current in the parasitic transistor goes with $1/L$). All test conditions and conventions used in the legend are the same as in Fig. 46. The DR, temperature, and bias conditions are comparable for all nodes. Note that the pre-rad I_{OFF} is largely determined by the specific "flavor" of the technology (low-power versus high-performance, for instance).

To understand if down-scaling of CMOS technologies has really brought any benefit in their TID tolerance, this section presents data collected over the last 30 years at CERN on commercial-grade technologies. Custom test structures containing individual transistors of different sizes have been integrated in different planar CMOS technologies in nodes ranging from 500 to 28-nm, from several manufacturers, then irradiated with X-rays, and measured under the same conditions. Figs. 46 and 47 show the resulting threshold voltage shift, normalized to 1 Mrad(SiO$_2$) of TID, for nMOS and pMOS transistors, respectively. Each data point refers to a different technology and is positioned along an x-axis representing the CMOS node. The dotted line is a guide for the eye for a decrease proportional to the square of the gate oxide thickness, in the hypothesis that this decreases linearly with the node size, to produce a plot similar to those in Figs. 5 and 6. Despite the relatively large error affecting the points of the most scaled-down nodes, for which ΔV_{TH} is so small that it is affected by systematic errors in the empirical procedure to extract V_{TH}, the results of wide and long transistors in Figs. 46(a) and 47(a) clearly illustrate the trend of continuously reduced sensitivity with down-scaling, for both full-SiO$_2$ and high-k gate stacks (introduced around 40-nm). The comparison with Figs. 46(b) and 47(b), on the other hand, powerfully shows how the TID response of narrow and/or short transistors is dominated by radiation effects in parasitic oxides. Because of RINCE and/or RISCE, due to the STI and the spacer oxides, ΔV_{TH} of narrow and/or short transistors is typically a full order of magnitude larger than for their wide and/or long counterparts in each of the measured technologies. Notwithstanding RINCE and RISCE, the degradation of the electrical properties of the transistors in the most recent nodes appears to be limited below what would induce failure in typical circuits exposed to hundreds of kiloradians or more. If TID-induced parametric variation of MOSFETs has decreased with down-scaling following the evolution of the gate stack, and in particular the thickness of SiO$_2$, the threat posed by the opening of leakage current paths is, in principle, still present. Indeed, as seen in Section II-C, radiation-induced leakage currents do not depend on the gate oxide. For this reason, in recent years, the failure of many commercial ICs during total dose tests has been determined by an excessive increase in the current consumption traceable to the opening of leakage current paths. However, this leakage

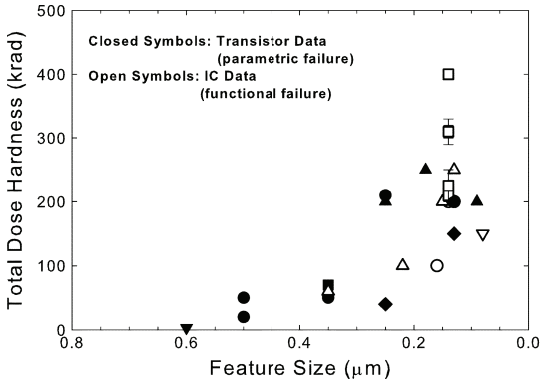


Fig. 49. Total dose to failure for digital circuits as a function of the CMOS technology node used for manufacturing the ICs. The data were compiled in 2010 from numerous articles in IEEE NSREC Radiation Effects Data Workshops and include measurements of both transistors and ICs. The evident trend is a sharp increase in the TID tolerance with down-scaling. (After [88].)

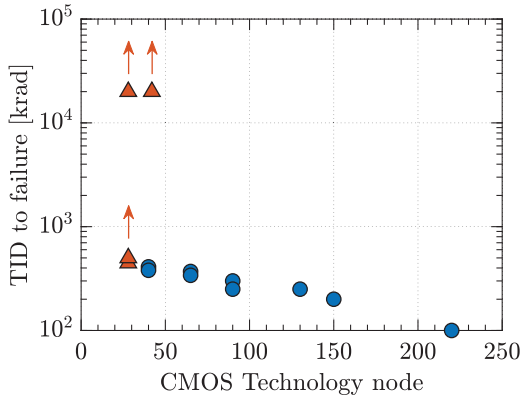


Fig. 50. TID to failure for Xilinx SRAM-based FPGAs manufactured in different CMOS technology nodes. Data are collected from a series of sources [192], [193], [194], [195], [196]. Red dots with arrows represent tests during which the circuit was still fully functional at the maximum TID reached in the test, so they are lower limits for TID to failure. Multiple points for the same node indicate multiple data sources—some of which explored a different TID range. (After [192], [193], [194], [195], and [196].)

is influenced by technological parameters such as the doping profiles, the quality of the STI (defect density) and its interface with the silicon, and the electric field across the STI. Once again, data from the 30-year-long CERN survey can be used to look for potential trends common to all technologies. Fig. 48 illustrates the resulting evolution of the drain-source leakage current with TID in nMOS transistors. In older technology nodes, the leakage current increase is observed at lower TID levels, 100 krad(SiO_2) or less, and reaches considerably higher levels than in more advanced nodes. The 65-nm transistors and below do not show relevant I_{OFF} at 1 Mrad(SiO_2), and 28-nm samples only exhibit a sensible—but limited—increase above 100 Mrad(SiO_2). This figure reveals a trend for a reduced impact of TID-induced leakage currents with the down-scaling of planar CMOS technologies.

The above results on both parametric shifts and leakage currents in transistors from manufacturers of CMOS technologies suggest a trend toward an increase in the TID tolerance of commercial ICs with down-scaling. A first confirmation of this hypothesis is visible in Fig. 49, taken from a compilation of data published in 2010 [88] and including technologies until the 90-nm node. This same trend, extended to smaller nodes, can also be observed in Fig. 50 for one of the most representative classes of complex logic circuits, SRAM-based field-programmable gate arrays (FPGAs). With the decrease of the gate oxide thickness related to down-scaling, the most frequent TID mechanism originating these failures is the increase of leakage currents that either brings the current supply beyond specifications or determines the loss of some of the circuit functionalities. The specificity of each circuit strongly influences the failure mechanism. In SRAM-based FPGA, for instance, leakage can lead to the corruption of the programmed bits determining the configuration of the circuit, thus leading to full loss of the intended functionality.

Although the measurements above include a large range of nodes from different manufacturers, the result can only be taken as a trend rather than a forecast for any past or future technology. Given that the radiation response is influenced by the details of the manufacturing process, there is no guarantee that devices in any and all planar CMOS technologies will be fully compliant with the trend illustrated above. As a powerful indicator of this aspect, the next section reports the examples of the measured variability in the radiation response of transistors fabricated by the same manufacturer in different plants (hereafter identified as "Fabs") or even in the same plant at different times.

B. Variability of the TID Response of Planar CMOS

Several studies have demonstrated that variations in the quality of oxides, their geometry [197], or the doping profiles [198] can lead to significant changes in the magnitude and dynamics of the TID response. More recent data in [199] evidenced a large fab-to-fab variability in the TID-induced leakage current of nMOS transistors in a 130-nm CMOS process [Fig. 51(a)]. The transistors used in this work are produced by the same manufacturer in three different fabrication plants, labeled as Fabs A, B, and C in the figure. While devices manufactured in Fabs A and B exhibit relatively small variation in leakage, nMOSFETs from Fab C show an increase in I_{OFF} of about four orders of magnitude. In the same work, a significant lot-to-lot variability was measured in TID-induced degradation of the maximum drive current I_{ON} of nominally identical minimum size pMOSFETs [Fig. 51(b)]. This variable TID response originates from differences in the details of the processing. Different fabs are often equipped with different machinery for the same processing steps, and while the electrical characteristics of the transistors are guaranteed to be identical, some physical details might be significantly different—this is particularly true for parasitic oxides like STI or spacers. The lot-to-lot variability can instead be due to normal fluctuations in most processing steps, again only leading to different defects in regions of the transistors that do not normally affect the electrical behavior. Here again, the rapid deposition of the isolation oxides can normally tolerate processing fluctuations without visible impact. These results demonstrate the impossibility, without testing and on

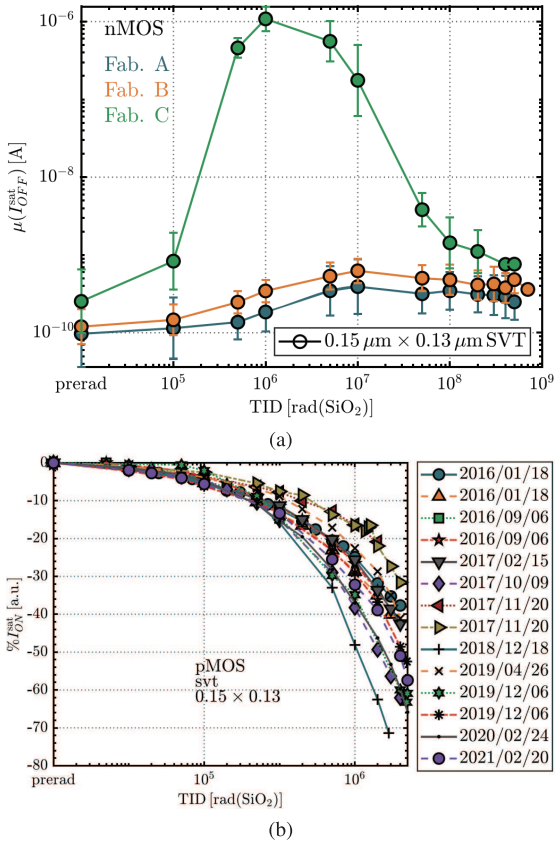


Fig. 51. (a) Fab-to-fab variability in the TID-induced leakage current of nominally identical nMOS transistors from a single manufacturer in a 130-nm technology. Samples from three plants, identified as A–C, were exposed to an X-ray source (40 kV, W target). I_{OFF} was measured with the maximum voltage applied to the gate and drain, $V_{GS} = V_{DS} = V_{dd}$. (b) Lot-to-lot (or run-to-run) variability in the maximum drive current (I_{ON}) degradation with TID of identical pMOS transistors produced by the same manufacturer in the same fab at different times. SVT stands for "standard V_{TH}" and the legend indicates the manufacturing time of the lot that the sample represents. (After [199].)

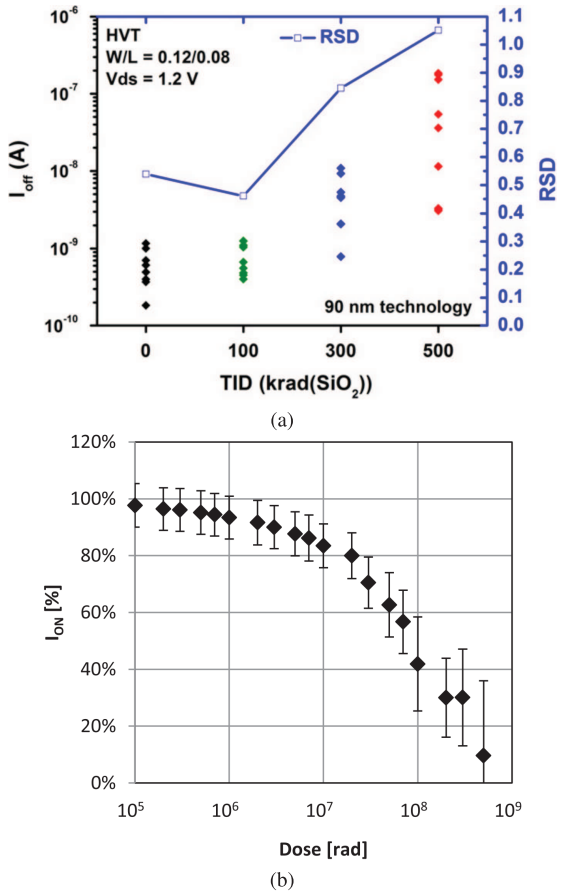


Fig. 52. (a) Within-chip variability of leakage current I_{OFF} for eight identical nMOS transistors in 90-nm CMOS technology. The relative standard deviation (RSD), i.e., the ratio of the standard deviation to the mean, increases for TID > 100 krad(SiO_2). (b) Within-chip variability of ON current for six identical pMOS transistors in 65-nm CMOS technology, indicated by the error bars, increases for TID ≥ 10 Mrad(SiO_2). (After [201] and [202].)

the sole basis of the trend illustrated earlier, concluding that circuits manufactured in any technology node have a conformal TID response. However, the existence of a trend can be usefully exploited, with due care, and suggests that many manufacturing choices are common across different CMOS technology nodes and suppliers.

In addition to fab-to-fab and lot-to-lot variability, total dose can also increase variability between nominally identical devices on the same chip (matching). Fig. 52(a) illustrates the impact of TID on the variability in leakage current for eight identical nMOS transistors in the same chip in a 90-nm CMOS technology. The distribution of leakage current values widens with increasing TID above 300 krad(SiO_2). Similarly, the transistor-to-transistor variability of the ON current increases for TID ≥ 10 Mrad(SiO_2) for the pMOSFETs in 65-nm CMOS technology reported in Fig. 52(b). Similar results have also been recently measured in FinFETs, in a 16-nm CMOS technology [200]. This variability is normally smaller than the one observable between transistors from different fabs or lots and suggests a limit in the uniformity of the local defect density that some processing steps can achieve.

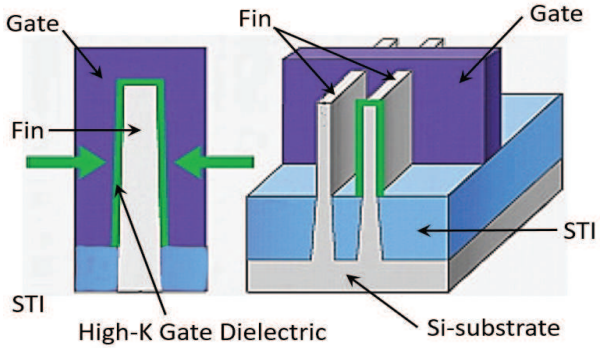


Fig. 53. Schematic of the FinFET with the thin gate oxide surrounding the "body" along the three sides. The representation refers to a bulk-FinFET technology, common in mass-market, where the fin is built on a Si substrate having a "neck" surrounded by STI oxide. (After [94].)

C. TID in FinFET Technologies

FinFET technologies have replaced planar CMOS starting with the 16-nm node. In FinFETs, the silicon "body" is surrounded by the thin gate oxide on three sides (see Fig. 53), which enhances the gate control on the channel. However, in bulk FinFET technologies, the channel fins are built on a

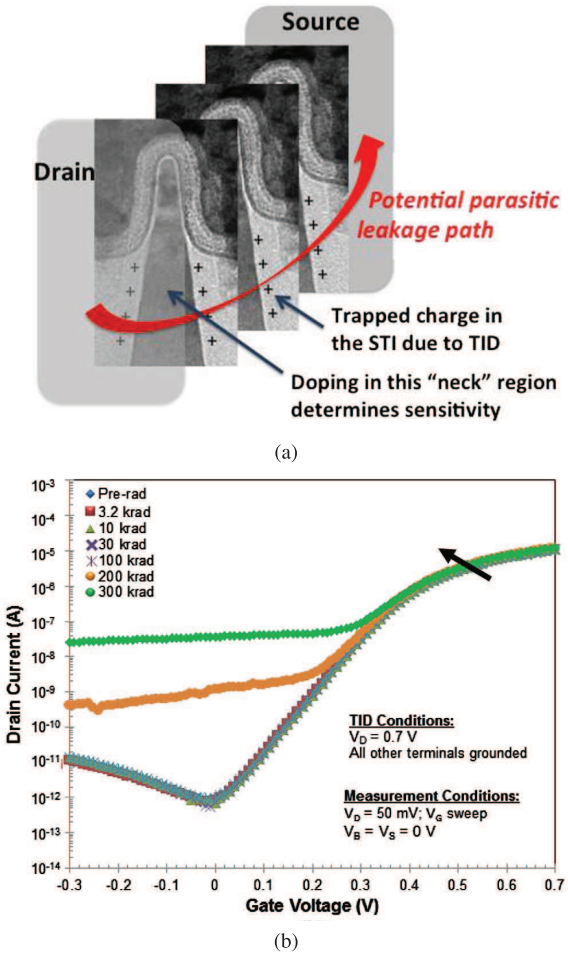


Fig. 54. (a) Illustration of the drain-source leakage path forming in the "neck" region of FinFETs because of TID-induced hole trapping in the STI oxide. (b) Experimental evidence of increase in drain-to-source leakage current induced by TID in an n-channel FinFET. (After [204].)

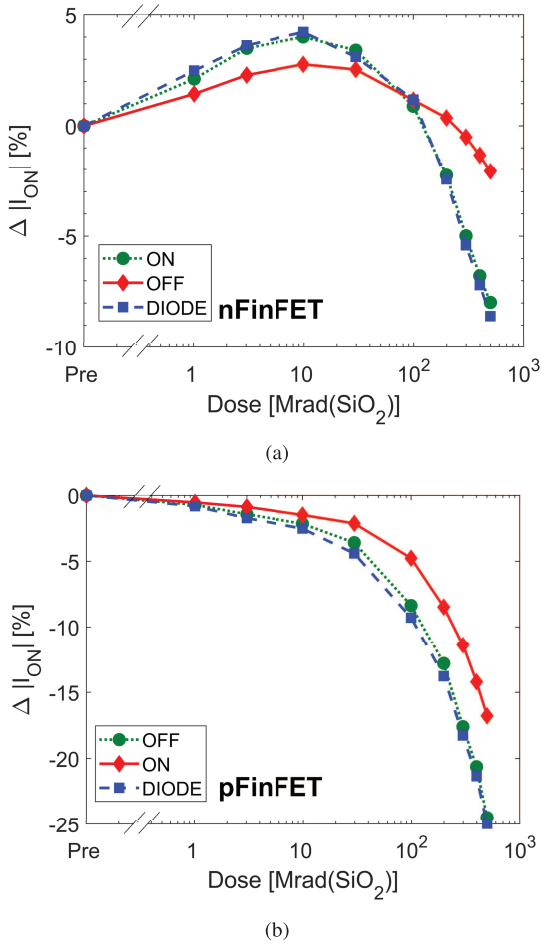


Fig. 55. Evolution of I_{ON} of (a) nFinFETs and (b) pFinFETs with L = 240 nm built in the 16-nm FinFET technology and measured at small V_{DS} (linear regime). Devices were irradiated in "DIODE" (V_{GS} = V_{DS} = V_{dd} = 0.9 V), "ON" (V_{GS} = V_{dd} = 0.9 V), and "OFF" (all terminals grounded) bias conditions during exposure. (After [94].)

silicon substrate with a bulk "neck" region surrounded by the STI oxide. In early experiments, this bulk neck region has been identified as a vulnerability to the TID resilience [94], [118], [203], [204]. Indeed, as shown in Fig. 54, positive charge trapping in the STI can lead to the opening of a drain-source leakage path in nMOS transistors, similar to planar technologies (discussed in Section III-A). The fabrication process may significantly influence the TID response in FinFETs; thus, currently extracting clear trends is challenging due to limited data availability stemming from the higher costs associated with FinFET technologies. Some of the published results from recent works studying commercial FinFET technologies are presented in this section.

A set of custom-designed test structures with individual transistors was used in [94] to study the TID response of a 16-nm technology up to 1 Grad(SiO_2). This FinFET process exhibits excellent resilience, with only a slight increase in I_{OFF} for nFinFETs, fully recovering after 24 h of annealing at 100 °C, and a worst-case decrease of about 25 % in I_{ON} for pFinFETs. The I_{ON} current in nFinFETs shows a "rebound," whereas it monotonically decreases in pFinFETs, as shown in Fig. 55 across all bias conditions during irradiation. These observations are explained with the model schematically illustrated in Fig. 56, where charge trapping in the STI or at its interface with silicon (in the "neck" of the FinFET) drives these effects. Given the positive polarity of trapped charges, the holes in the channel of pFinFETs are steadily "repelled" with increasing dose and the interface with the STI gets depleted. In nFinFETs transistors, holes trapped in the STI dominate the response at both low and high doses, extending the channel area in the bulk neck region. However, at ultra-high doses, the latent build-up of interface traps in the shallow neck region reduces the effective channel size (resulting in lower I_{ON}) while maintaining a leakage current path deeper in the fin neck [205]. Recent experimental results, combined with TCAD simulations, identify non-uniform charge trapping in the STI oxides, specifically in two different sensitive regions [205]. The first involves rapid positive charge trapping in the sidewalls, which primarily causes a monotonic increase in leakage current. The second involves interface trap formation in the upper corners of the STI, which reduces the transconductance by lowering the effective channel height (i.e., the effective channel width) [205]. This reduction in effective

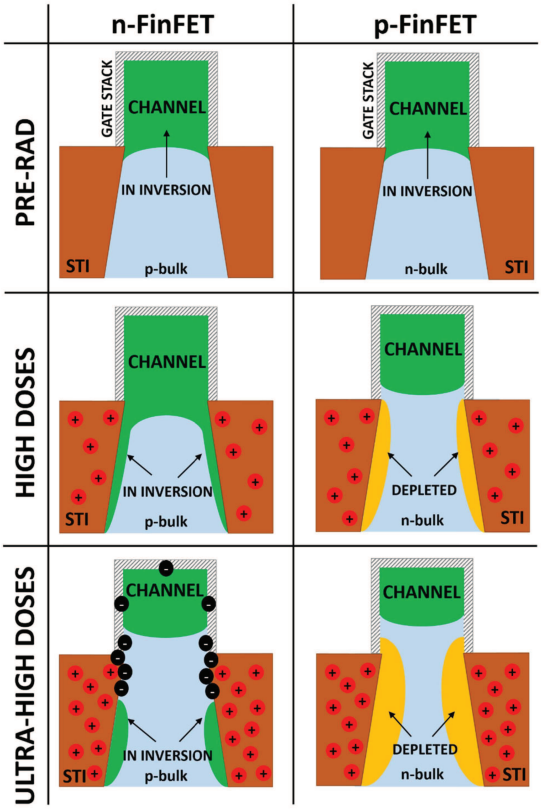


Fig. 56. Schematic of the phenomena behind the radiation response of FinFETs in the 16-nm technology. The view is a vertical cut-plane normal to the channel fin, similar to the one shown in Fig. 53. TID-induced effects are illustrated when devices are biased in inversion (V_{GS} = 0.9 V) at high (~1 – 10 Mrad(SiO_2)) and ultrahigh doses (>10 Mrad(SiO_2)). The green-colored regions are inverted regions of the Si bulk, while the yellow-colored ones identify those where the n-bulk of pMOSFETs is in accumulation ("depleted" in the context of the original paper meant not-inverted). Positive trapped charges are indicated with "+," while "–" indicate the interface traps that are negatively charged in the case of pMOS transistors. (After [94].)

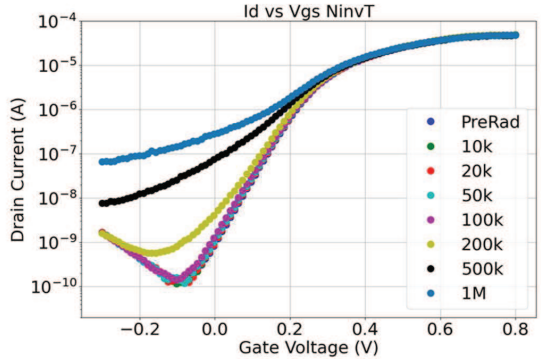


Fig. 57. Transfer characteristics of nFinFETs in the 12-nm node exposed to TID with an X-ray source up to 1 Mrad(SiO_2). The bias applied during irradiation was the "ON" bias, with V_{GS} = 0.8 V and all other terminals grounded. The only relevant effect is the increase of the drain-source leakage current in the subthreshold region. (After [208].)

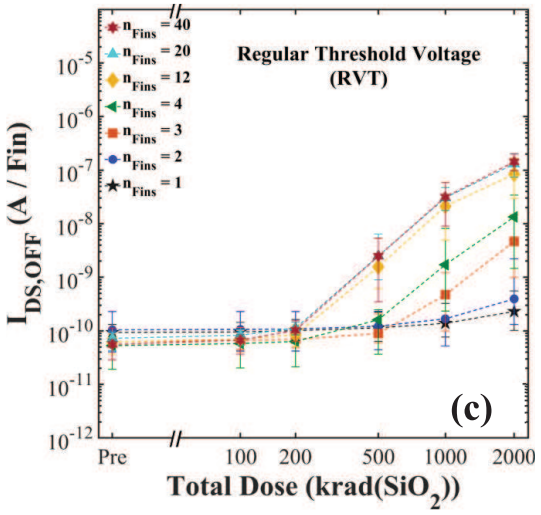


Fig. 58. Evolution of the drain-source leakage current per Fin in transistors fabricated with the GF12LP 12-nm FinFET technology with regular-V_{TH}. Transistors with a high number of Fins evidently show a larger increase in I_{OFF} per Fin. (After [209].)

channel width is similar to what has been described for planar technologies in Section III-E, where the upper corners of the STI oxide play a crucial role in charge trapping [152]. Additionally, similar to the influence of halo implantation in planar transistors (Section III-D), halo implantation improves the tolerance of short-channel transistors, and devices with minimum gate length (16 nm) are less affected by TID than those with L = 240 nm [94]. Conversely, no effect related to charge trapping in the spacer oxide has been reported for either this 16-nm or other FinFET technologies.

TID tests were also performed in the 14-nm node [206], [207]. Although published four years apart without disclosing the manufacturer, it seems very likely that both studies examined the same process. The earlier results [206] evidence a significant increase in drain-source leakage current in nFinFETs, while the more recent publication shows almost no change in the subthreshold region. This discrepancy is challenging to explain solely based on the differing study conditions, such as applied bias, gate length, and transistor type, suggesting that it may be attributed to process modifications introduced between the two studies or natural variability.

Several interesting results have emerged from a commercial 12-nm FinFET technology (the GF12LP). Transistor measurements up to an accumulated TID of 2 Mrad(SiO_2) evidenced minimal impact on the transfer characteristics of both nFinFETs and pFinFETs [203], [208], [209]. However, a significant drain-source leakage current in nFinFETs was observed above about 200 krad(SiO_2), as shown in Fig. 57. The magnitude of the leakage current varied based on the transistors' characteristics, including the "flavor" (regular-, low-, or high-V_{TH}) and the number of parallel fins. The dependence on the initial threshold voltage was attributed to the doping profile in the fin, which affects the status of the silicon interface with the STI (accumulation, depletion, or inversion) [209]. The variation related to the number of fins was more pronounced, as illustrated in Fig. 58; the TID-induced leakage per fin increased with the number of fins. This variation was initially attributed to different stress levels in the STI oxide during manufacturing, resulting in variations in defect precursor density or electric field within the STI, both of which contribute to trapped

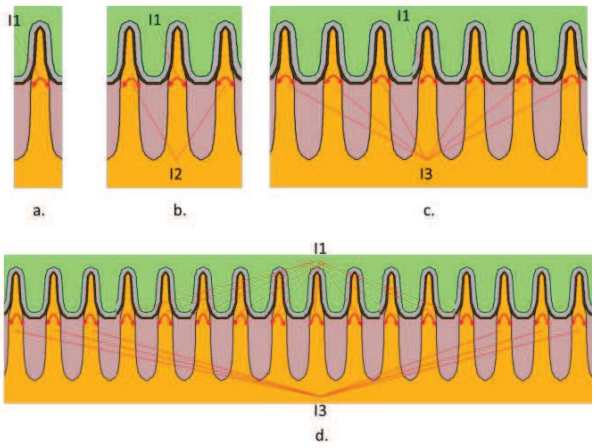


Fig. 59. Model proposed in [209] for fitting correctly the larger leakage visible in multi-Fin transistors. The figure shows the cross section of several FinFETs with a variety of fins. The model is based on location-specific leakage currents. (a) 1-fin transistor showing the smallest parasitic current, I1. (b) 3-fin transistor showing I1 (interior fin), and I2 (two outer fins). (c) 7-fin transistor, showing I1 (interior fin), and I3 (three outer fins on each side). (d) 16-fin transistor, showing I1 (10 interior fins), and I3 (three outer fins on each side).

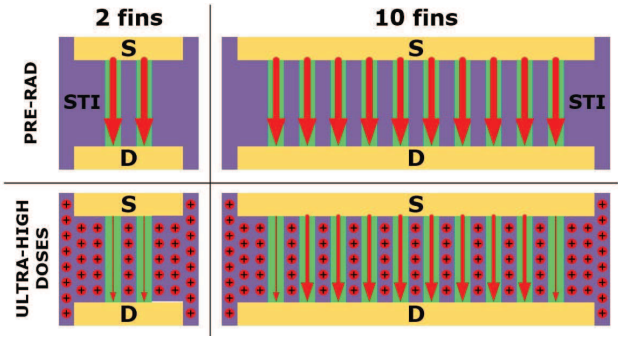


Fig. 60. Model proposed in [210] explains the more significant I_{ON} degradation of pMOS FinFETs with a lower number of Fins. Transistors were fabricated in 16-nm technology and irradiated at ultra-high TID. This model posits that more charge is trapped in the thicker STI oxide at the edge of the multi-Fin devices. The thickness of the arrows in each Fin represents the magnitude of the drain-source current. In a multi-Fin transistor (right), only the two peripheral Fins have thick-STI borders with higher trapping, resulting in less degradation per fin compared to the two-Fin transistor (left). (After [210].)

charge build-up during irradiation. The model proposed in [209] suggests that leakage current in each fin depends on its surroundings; isolated fins or those surrounded by more than three fins on each side exhibit lower leakage, while the outermost three fins on each side of a multi-fin transistor experience the highest leakage, as schematically depicted in Fig. 59. Recently, another publication by the same research group proposed a different explanation related to the trapping of negative charge in the SiN layers introduced close to the lateral STI in this specific technology node. This model is thus compatible with the opposed observation—larger degradation in transistors with a smaller number of parallel fins—in a previous publication studying FinFETs in a 16-nm technology [210]. In this case, the degradation concerned the I_{ON} of pMOS transistors irradiated to ultra-high TID levels. The explanation proposed in that paper relied on the fact that the STI oxide

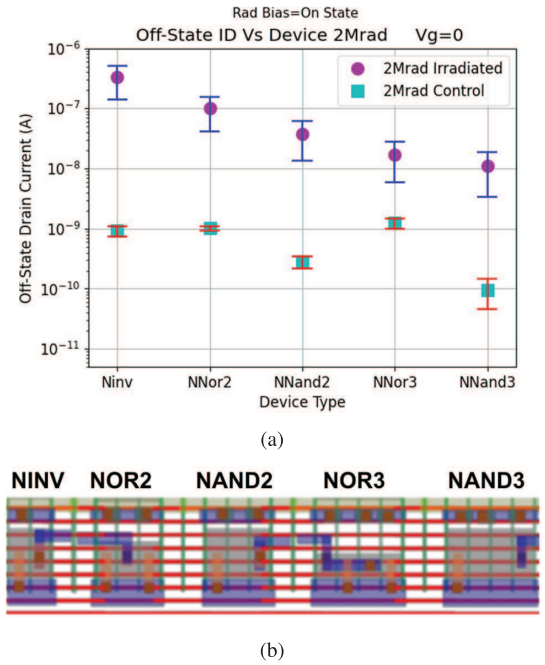


Fig. 61. (a) TID-induced I_{OFF} increase of transistors in logic gates in 12-nm FinFET technology correlates with (b) geographical location of the gates in the design. Symbols represent the average values calculated from ten measurements (two devices across five chips) for the irradiated data and four measurements (two devices across two chips) for the controls (fresh devices). (After [203].)

separating two fins is much thinner than the one situated at the periphery of the multi-fin transistor. As qualitatively illustrated in Fig. 60, TID-induced charge trapping is much larger in the thicker periphery oxide; thus, fins at the periphery of the multi-fin device are more significantly affected by radiation.

Another notable result highlighting the complexity of the radiation response in FinFETs was presented in [203]. In this study, I_{OFF} of n-channel 14-nm FinFETs in logic gates varied based on the geometrical location of the gate within the test structure after exposure to TID levels up to 2 Mrad(SiO_2). As shown in Fig. 61, post-TID leakage current decreases from left to right, a pattern consistently observed across different test sites on the silicon wafer. These differing radiation responses were explained by the slight gradient variations in doping within the sub-fin region, resulting from the specific layout of the overall design [203]. To support this, they presented TCAD simulation results, indicating that small changes in sub-fin dopant concentration did not significantly affect the pre-radiation transfer characteristics but greatly influenced the post-radiation drain-source leakage current.

The results above in the 16, 14, and 12-nm nodes reveal an increased complexity in the response of FinFETs to TID with respect to older planar technologies. Other than the transistor size [211], which already influenced planar CMOS TID-induced degradation, additional geometric characteristics—such as the number of fins and their spatial arrangement—play a significant role. A key challenge remains in distinguishing whether these effects stem from the unique

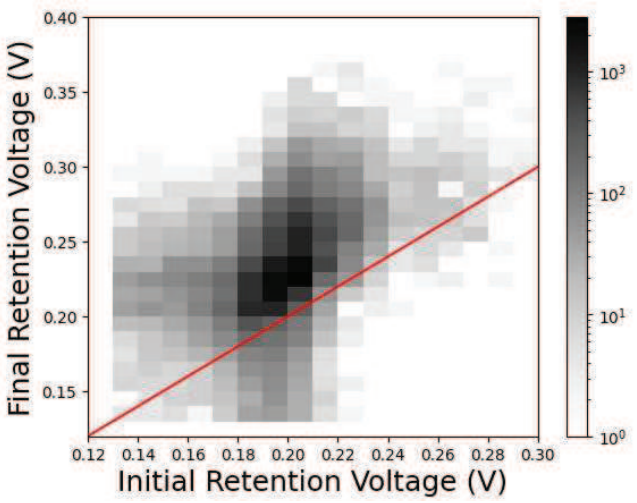


Fig. 62. Results from X-ray irradiation of a 256 kbit dual-port SRAM fabricated with 5-nm FinFET technology. After exposure to 1 Mrad(SiO_2), an increase in variability and the retention voltage V_{DR} is visible. Cells were tested at a nominal voltage of 750 mV with an all-0 data pattern. The red line indicates the expected position for cells with identical pre- and post-irradiation V_{DR}. (After [215].)

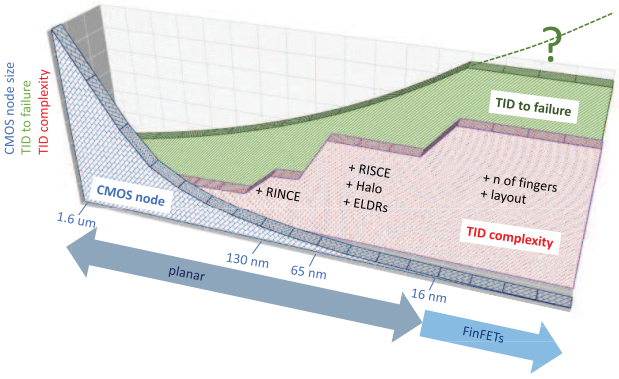


Fig. 63. Schematic of the trends observed in planar and FinFET technology nodes: both the TID tolerance and the complexity of the mechanisms have generally increased. With the limited available data, it is unclear if the trend for increased TID to failure continues in FinFET technologies. The abrupt steps in the "TID complexity" indicate the approximate technology node where the listed effects have initially been observed. Important caveat: these trends are representative of typical responses but are not all-inclusive; testing is still required to determine the tolerance of specific technologies and ICs.

characteristics of FinFETs themselves or are simply a result of scaling to dimensions below the 20-nm threshold.

Published data on technologies below 10 nm are rare due to their limited accessibility and very high cost. In particular, data on the response of individual transistors are missing. Two studies [212], [213] have presented TID results on ring oscillators (ROs) fabricated in a 7-nm commercial process. These oscillators used transistors with two fins. Measurements of delay-per-gate and current consumption of ROs exposed to X-rays up to 380 krad(SiO_2) showed that all parameters varied by less than 1 %, indicating a good level of TID tolerance. The other two papers investigated the radiation response of a 5-nm FinFET technology using an SRAM circuit as a test vehicle [214], [215]. One study [215] focused on the TID-induced shift of the data retention voltage V_{DR} in single- and dual-port 256 kbit SRAMs. V_{DR} was determined by sequentially writing a data pattern at the nominal voltage (750 mV), storing the data at a lower voltage V_{store}, and then reading it back at nominal voltage. The minimum V_{store} required for successful read-back defined V_{DR}. After exposure to a TID of 1 Mrad(SiO_2), the pre- and post-irradiation V_{DR} values were compared (Fig. 62). While some SRAM cells exhibited a decrease in V_{DR}, most showed an increase, particularly in dual-port cells. The average increase was limited to tens of millivolts, but a large variance was observed with peaks of up to 150 mV in some cells. This variability makes it difficult to predict the V_{DR} change for each cell, suggesting that TID exposure could substantially affect the lowest operational supply voltage for SRAM arrays at this technology node. The second paper from the same researchers reported an increase in current consumption of the SRAM and other connected test circuits during X-ray irradiation up to 150 Mrad(SiO_2). Current consumption rose up to about 10 Mrad(SiO_2) then began to decrease, eventually falling below the nominal levels (for as-fabricated devices) by the end of the exposure, while all circuits remained functional. This behavior aligns with trends observed in the leakage current of many planar technologies described in III-A, suggesting that similar mechanisms involving the dynamics of oxide trapped charge and interface traps in the STI oxide may be at play in this advanced FinFET technology as well.

VII. Conclusion

The down-scaling of CMOS technologies in the last decades had a significant impact on the reliability of ICs in radiation environments. In particular, the accompanying decrease in the gate oxide thickness progressively improved the transistor tolerance to TID-induced effects. Starting from gate oxide thicknesses of 5 nm, parametric shifts related to charge trapping in the gate oxide became comparable or smaller than the parametric dispersion due to manufacturing, even at multi-Mrad dose levels. Consequently, effects related to defect accumulation in other oxides surrounding the transistors have become visible and sometimes dominate the radiation response of devices. The well-known drain-source and inter-junction leakage currents become the main reasons for functional failures due to TID. Narrow-channel effects (RINCE), also due to radiation effects in the STI oxide, were observed starting from the 180 to 130-nm technology, in some cases modulated by the presence of the HALO implants. Short channel effects (RISCE), initially reported in the 130- and 65-nm nodes, were attributed to trapping in the spacer oxide used for the LDD implant. Because of the low quality of these deposited oxides and the low-intensity electric field across them, charge accumulation appeared to be truly dependent on the DR used for irradiation, evidencing ELDRS, similar to the one observed in linear bipolar circuits. The situation is conceptually represented in Fig. 63: a trend for an increase in TID tolerance with down-scaling has been observed in planar CMOS processes, while the complexity of the radiation response also grew.

The transition to FinFETs at the 16-nm node promised a further improvement of the natural radiation tolerance of CMOS circuits because these novel transistors are almost fully surrounded by a thin gate oxide. However, large-scale production revealed that such leakage currents could still occur. Moreover, minute details specific to every individual transistor, such as the number of parallel fingers or spatial relationships to neighboring transistors, also sensibly contributed to influence its TID sensitivity, thus further increasing the complexity of the TID effects. The lack of extensive data in these expensive technologies of difficult access still eludes a conclusive statement concerning their relative tolerance with respect to their planar forbears. So far, the trend of enhanced TID robustness with downs-scaling appears to extend to FinFETs, accompanied, however, by an evident rise in the TID response complexity. The future trends depend on the technological choices of the largest semiconductor manufacturers. Transistor implementations such as in gate-all-around FET technologies, which feature a thin gate oxide fully enclosing a small conduction Si "tube," are expected to practically eliminate any TID-related vulnerability. However, as already seen in the past, the successful mitigation of TID effects will still be tributary to the details of the fabrication process in commercially viable technologies. The effort of test and qualification for applications in a radiation environment will therefore need to be continued in the foreseeable future.

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